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Design of the Power Control Module of TD-SCDMA in Fast Fading Channels

By

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Abstract:

Power Control is essential for CDMA based Mobile Communication Systems. Power Control treats the near far problem, enhances the coverage and the capacity and overcomes fading. Adaptive Power Control improves the system performance in case of severe fading conditions. This paper considers the design of the Power Control module of TD-SCDMA system in fast fading condition. A closed loop adaptive step size power control algorithm is suggested. The proposed power control module can be easily implemented within the TD-SCDMA chipset.

Keywords:

CDMA, fast fading, TD-SCDMA and power control.

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1. Introduction:

TD-SCDMA system has been presented by CCSA (China Wireless Communication Standards Organization) and has already become the 3G (3rd Generation) wireless communication standard of ITU (International Telecommunication Union) [1]. The TD-SCDMA system [2], [3] inherently has the characteristics of both Code Division Multiple Access (CDMA) and Time Division Multiple Access (TDMA), with up-link (reverse-link) synchronization, a software radio, and a smart antenna [4], to increase channel capacity and improve bandwidth efficiency.

Power control is a means primarily designed to compensate for the loss caused by propagation and fading. Power control has in particular been reported to be crucial for the performance of the time division code-division multiple-access (TD-CDMA) system.

Power control is needed for both forward and reverse channels. Forward link power control is considerably less complicated than reverse link power control. In TD-CDMA systems reverse link power control is also more crucial and sensitive in the sense that power levels received at the base station from different mobile units should be roughly equal, so that no single mobile unit can dominate and prevent recovery of signals from other mobile units. This work considers reverse link power control.

Power control can employ either an open loop [5] or a closed loop [6-8]. In closed-loop power control, the base station uses the quality of the signal received from a mobile unit to issue a command to tell the mobile unit how to adjust its transmitted power. In open-loop power control, each mobile unit adjusts its transmitted power assuming that path losses in both directions forward and reverse, are symmetric. Open loop control can only compensate for the loss due to long-term fading, and it cannot make up for the loss due to short term fading. Since closed-loop power can be adjusted through feedback and it also performs better to compensate for both long- and short-term fading. Closed-loop power control is studied in this work.

According to the information measured to determine whether to raise or lower the transmitted power from a mobile unit, power control is divided into two categories: strength based, e.g., [5], and signal-to-interference-based (SIR-based), e.g., [5], [7]. In strength-based schemes, the strength of a signal arriving at the base station from a mobile unit is measured to activate proper power control action, whereas in SIR-based design, the quantity measured is SIR, with the interference consisting of both channel noise and multiuser interference. SIR is clearly a more accurate indication of signal quality and provides better performance. However, SIR-based power control may cause positive feedback, which can endanger the stability of the system. One method to make the loss of this deficiency is to have strength-based and SIR-based power control schemes combined [9]. In TD-SCDMA system, Dedicated Physical Channel (DPCH) uses the TPC (Transmit Power Control) symbol in Physical Layer (L1) to conduct

closed loop power control for uplink and this closed loop control is SIR-based situation. In this work, we study an adaptive power control algorithm based on fixed step size algorithm. Because the fixed step size method has invariant adjustment amplitude, it may not catch on the power alteration rapidly under fast fading but the adaptive method can adjust the step dynamically according to the characteristic of fast fading channel thus gain better control effect.

The rest of this paper is organized as follows. Section 2 presents the process of the closed loop adaptive power control algorithm for uplink. Section 3 introduces implementation of the power control module of TD-SCDMA in fast fading channels. Simulation results showing the improvements achieved with the proposed adaptive power control algorithm with respect to the fixed step size one is discussed in Section 4. Finally, summary and conclusion are given in Section5.

2. Closed Loop Adaptive Power Control Algorithm for Uplink:

Closed loop power control is the kernel of uplink power control and it is accomplished by mobile units with the assistant of base station [1]. The base station detects SNR of reverse business channel every 1.25ms, and then compares it with a certain threshold. If the received SNR is higher than the threshold value (written as SNR_thre in below), the base station will send an order to mobile units to reduce their launching power, otherwise increase their launching power, while mobile units adjust launching power every 1.25ms with step size 1dB usually. When mobile units cannot receive TPC bit because of losing synchronism, the launching power will remain in certain value. Also when base station cannot detect SNR without synchronism, the TPC command will be set “increasing” during this period. The fixed step size algorithm is carried out every frame, and the changing of SNR_thre is depending on the comparison result of current Frame Error Rate (FER) and frame error rate threshold (FER_thre). If FER is bigger than FER_thre, the error frame may be caused by current error frame or previous error frame, which is different situation and needs discussion respectively. Since the space is limited, we won’t give any further analysis.

Regarding closed loop adaptive power control for uplink, the process of this algorithm is quite simple and we can show it has a better performance than fixed step size algorithm in the following text. The key conception of our method is to be indicated as follows:

Suppose the number of tapping point of Rake receiver [10] in data receiving is L, and then the total receiving power P_R is:

$$P_R = \sum_{i=1}^{L} (P_{R,i}) \qquad (1)$$

where $P_{R,l}$ is the receiving power of the l^{th} tapping point.

Now we use a shift register in the receiver to deposit power control bits, on which we depend on regulating the power-adjusting step size adaptively. First, we define that the bit information be 1 or 0, if the receiving power P_R is smaller or bigger than the target power P_{target}. There is a 7 bit shift register storing the values of current and 6 previous power control bits, which is written as $R_0, R_1,\ldots, R_6$ in sequence. When there is 1 or 0 alternately, it means the receiving power is approximate to the target power. When there is 1 or 0 continuously, the step size needs adjusting strongly, for the receiving power is much smaller or bigger.

Assume step size weighting factor is g, ϕ is original step size and Δ is new step size, then Δ is

$$\Delta = \phi + g\,\lambda \qquad (2)$$

where λ is a system parameter. The corresponding relationship of $R_0, R_1,\ldots, R_6$ and g is scheduled in Table 1.Under other circumstance g is always 0 and when fading is slow, let $\Delta = \phi$. In fast fading situation, according to the values of $R_0, R_1,\ldots, R_6$ we can easily find g in table 1 and calculate step size in using equation (2).

Table (1): *Corresponding relationship of R and g*

R_0	R_1	R_2	R_3	R_4	R_5	R_6	g	g_1	g_0
1	1	1	0	X	X	X	1	0	1
1	1	1	1	0	X	X	3	1	1
1	1	1	1	1	0	X	2	1	0
1	1	1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	0	0	0
0	1	1	1	1	1	1	3	1	1
0	1	1	1	1	1	0	2	1	0
0	0	1	1	1	1	1	3	1	1

0	0	0	1	1	1	1	2	1	0
0	0	0	1	X	X	X	1	0	1
0	0	0	0	1	X	X	1	0	1
0	0	0	0	0	1	X	2	1	0
0	0	0	0	0	0	1	0	0	0

3. ***Implementation of the power control module of TD-SCDMA in fast fading channels:***

The main function of power control block is to maintain communication quality with as little as power loss thus decrease interference mutually in network and prolong the utility tie of terminal batteries. This model block can generates power control command and current power control bits information. In this paper we give simulation of closed loop power control for uplink, and it is SIR-based scheme to investigate system performance of BER and SNR. As seen in Fig. 1, after adding power control bits information, data source should judge how to adjust launching power and then pass it through Rayleigh Channel. Receiving end not only gets data but receives power control bits to decide TPC command and then gives sub-block calculating launching power a feedback. On the other hand, receiving end computes SIR and compares it with target value to generate new power control bits information. Without considering bit error amount, SIR-based closed loop power control model is simplified as shown in Fig. 2.

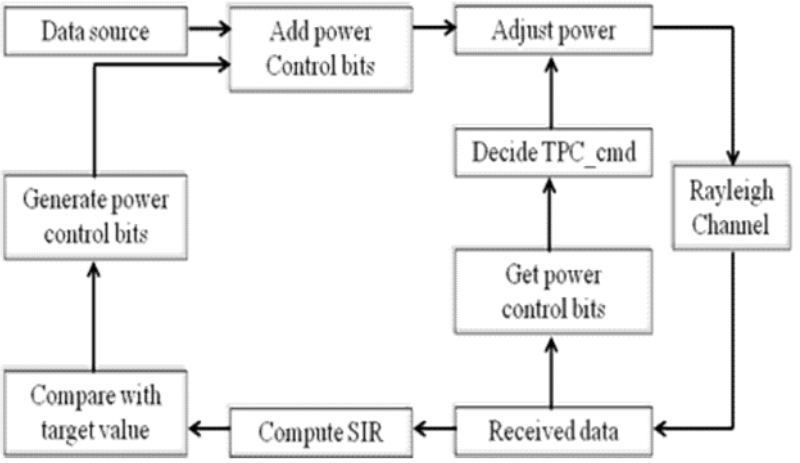

***Figure (1)**: SIR-based closed loop power control model*

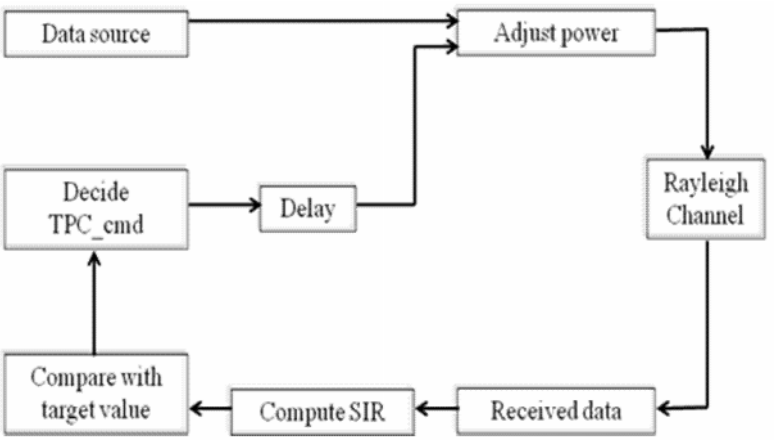

***Figure (2)**: Simplification of Fig.1 without considering bit error amount*

The implementation of adjust power block is illustrated in details in Fig.3, as shown the power control bits are received sequentially through the serial I/P of the first 7 bit shift register ($R_0, R_1,\ldots, R_6$), so we are able to store the last decided PCBs, on the –ve edge of the clock the PCBs are latched to be stable during the data processing by the next combination logic circuits (Decoder, AND/ OR gates), the 7×128 decoder actually do the physical mapping of the received PCBs into their corresponding g-value (represented by two bits g_0 and g_1. From table no.1, we obtain the g_0 and g_1 equations as follows:

$$g_0 = D_7 + D_8 + D_{15} + D_{16} + D_{63} + D_{124} + D_{126}$$

$$g_1 = D_{15} + D_{31} + D_{32} + D_{62} + D_{120} + D_{124} + D_{126}$$

The g value is latched by using two D-FFs and converted into analog value by the D/A converter. Then to obtain the Δ value in equation no.2, the g-value is multiplied by λ parameter and added to ϕ .

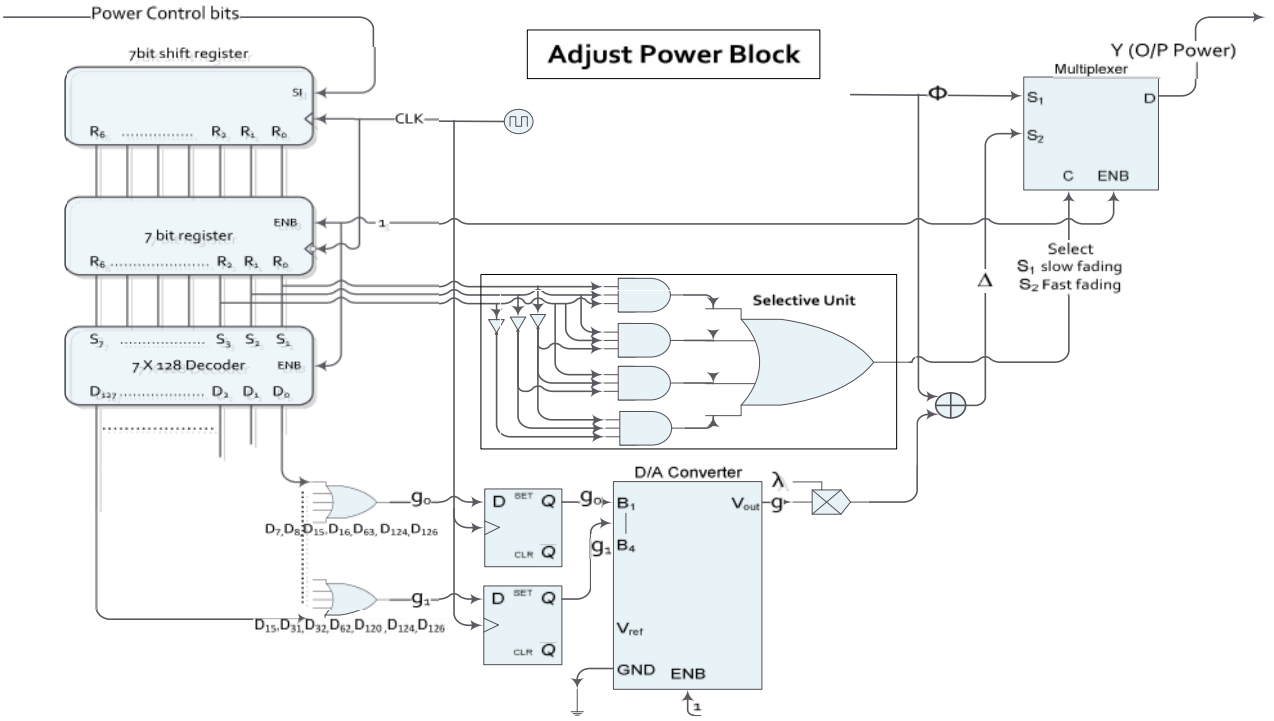

***Figure (3)**: Adjust power block diagram*

The selection unit is the most important part in the circuit, it enable us to decide either to add ϕ (Fixed Step Size) during slow fading or Δ (Adaptive Step Size) during fast fading, this selection is based on the last three received power control bits as shown by table 2, it was noticed from the table that the fast fading conditions are restricted to four possible versions implemented with different four AND gates, if the O/P of the OR gate is one fast fading parameter Δ is selected, otherwise slow fading parameter ϕ is selected that is done by the multiplexer as shown in Fig.3.

***Table (2):** four possible cases for fast fading*

R_0	R_1	R_2
1	1	1
0	1	1
0	0	1
0	0	0

4. <u>Simulation Results</u>

In this section we show the convergence improvement using the new APC algorithm. In figure 4, we show the system improvement between the proposed adaptive step-size algorithms and fixed step-size algorithms that ASPC is reached faster than FSPC that make the system is reliable and very minimum drop shot power and no over shot power that makes the system is able to maximize the capacity and to be green technology system in terms of energy savings.

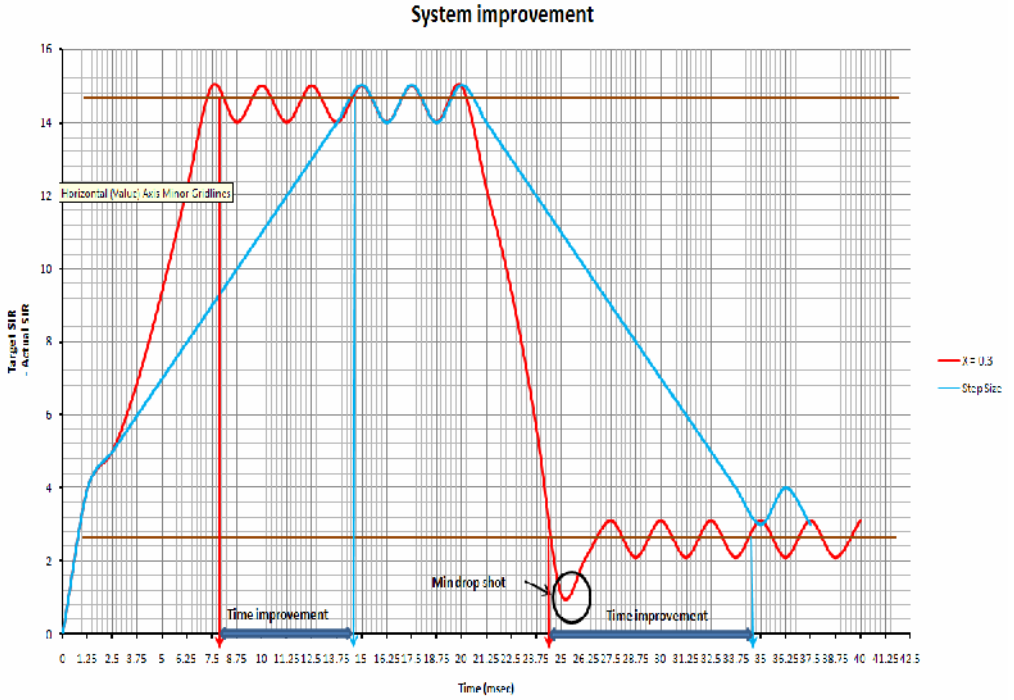

***Figure (4)**: Comparison of the SIR to SIR target convergence between fixed step and adaptive step power control methods.*

5. Conclusions:

This paper considers the design of the power control module of TD-SCDMA in fast fading channels. In case of no fading, power control bit will fluctuate and keeps the output transmitter power constant. In the case of fast fading, the optimum choice of the parameters and the adaptive step size algorithm considered will adjust the power very fast. The designed power control module can be easily implemented within the TD-SCDMA chipset.

References:

[1] Miaoyin Wang, Fei Ji and Gang Wei, "Simulation Analysis of Adaptive Power Control Method in TD-TCDMA System", IEEE, April 2007.

[2] http://www.3gpp.org/

[3] Ji Young Yunyz and Dan Keun Sung, “Joint Detection for On/Off Uplink Traffic in the TD-SCDMA System”, IEEE

[4] DALLAS SEMICONDUCTOR, "TD-SCDMA Radio Chipset Block Diagram for Handset Application", JUN 2001

[5] "Concepts in CDMA" in The CDMA Network Engineering Handbook, vol. 1, Qualcomm, Mar. 1993, chs. 4 and 8.

[6] S. Ariyavisitakul and L. F. Chang, "Signal and interference statistics of a CDMA system with feedback power control," IEEE Trans. Commun., vol. 41, pp. 1626–1634, Nov. 1993.

[7] S. Ariyavisitakul, "SIR based power control in CDMA system" in Proc. IEEE GLOBECOM Orlando KL, Dec. 1992, pp. 868-873.

[8] M. L. Sim and E. Gunawan, "Characteristics of closed loop power control algorithms for a cellular DS/CDMA system," IEEE Proc.-commun.,vol. 145, Mo. 5, Oct. 1998.

[9] Yu-Jun Yang and Jin-Fu Chang, "A Strength and SIR Combined Adaptive Power Control for CDMA Mobile radio channels" *IEEE Trans Veh Technol*, 1999, 48:1 996-2 004.