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Design and Implementation of Digital Delay Line Integrator (DDLI) using FPGA and DSP

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Abstract

In the present work, the design and implementation of digital delay line integrator (DDLI) which is a common radar signal processing technique is proposed. The design and implementation is achieved using two of the new developed digital hardware platforms: Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGAs). Comparison between these developed digital hardware platforms based on the implemented DDLI is introduced. This is done to find out the aspects of choosing which platform is the best for implementing certain radar signal processing technique.

I. Introduction:

The main objective of any radar system is to detect and locate targets of interest which usually are immersed in different unwanted signals such as noise, clutter, and jamming. These interferences degrade the ability to detect targets and must be reduced compared to the desired received signal in order to achieve reliable detection.

Generally, target detection would be an easy task if the echoing objects were located in a clear or empty background. In such a case, the echo signal can simply be compared with a fixed threshold, and targets are detected whenever the signal exceeds this threshold. In real radar applications, the target practically always appears in a background filled (mostly in a complicated manner) with point, area, or extended clutter. Frequently, the location of this background clutter is additionally subjected to variations in time and position. Therefore, degradation of the detection is occurred. Different radar signal processing techniques are used to overcome these problems and enhance the signal to noise (S/N) ratio [1].

The implementation of these techniques may be achieved using two of the new developed digital hardware platforms, FPGA and DSP. DSP processors are a specialized form of reprogrammable microprocessor, while FPGAs are an uncommitted sea of logic gates that may be reconfigured according to the application requirements

In this paper, design and implementation of Digital delay line integrator (DDLI) as one of the common radar signal processing techniques using DSP and FPGA is introduced.

Simulation is performed to clarify the difference in using both platforms and their advantages and disadvantages. This is done in order to answer the question of which platform is the best for implementing certain radar signal processing technique.

The rest of this paper is organized as follows; section 2 gives a general description for the design and implementation of the DDLI. Section 3 presents the design and implementation of the recursive DDLI using DSP. Design and implementation of the same DDLI using FPGA is presented in section 4. The conclusion comes in section 5.

II. Design and Implementation of the Recursive DDLI

There are two approaches for implementing DDLI: recursive and nonrecursive. The implementation of recursive DDLI shall be chosen for its simplicity and because it contains most digital operations used in digital design (addition, multiplication and delay). The derivation of the recursive DDLI starts from the analog one shown in Fig. 1. [2]

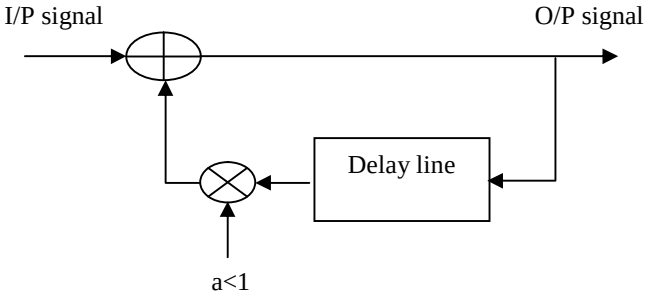


Fig. 1 The block diagram of the recursive delay line integrator

Replacing the delay line by a shift register with length L given by

$$L = \frac{T_r}{T_s} \quad (1)$$

where

L is the number of samples during the pulse repletion period T_r

T_s is the sampling period

The recursive DDLI transfer function becomes

$$\mathbf{H(z) = \frac{1}{(1 - aZ^{-L})}} \quad (2)$$

The multiplier, a, affects the performance of the delay line integrator. For a=1, the recursive integrator is ideal, but it is marginally stable. In this case, the integrator improves the signal to noise ratio N-times, where N is the number of integrated pulse during one beam. The stabilized integrator in Equation (2) improves the S/N ratio m-times.

Where m is found to be: [2]

$$m = (1 - a^N)^2 \times \frac{1 + a}{1 - a} \quad (3)$$

The implemented recursive DDLI is designed to integrate the video analog echo signal of a typical radar system with the parameters as shown in Fig. 2 (a).

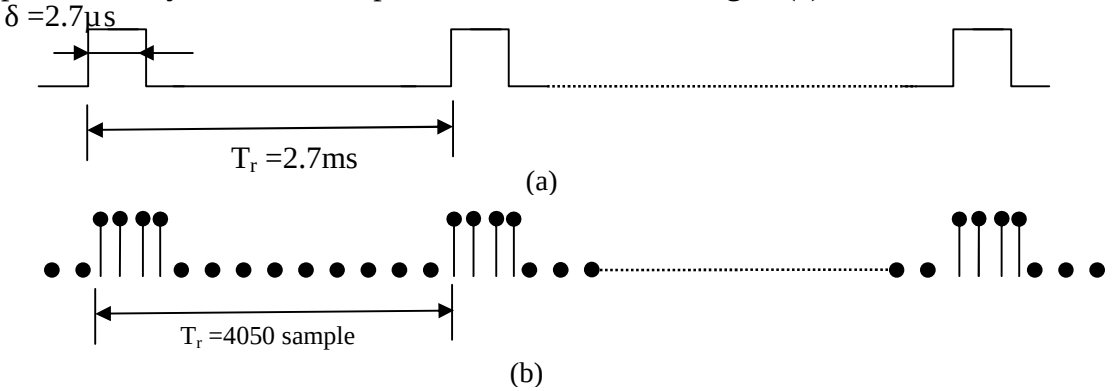


Fig. 2 Ideal echo video signal (a) analog form. (b) digital form.

This video signal is fed to analog to digital converter (ADC) to produce a 6 bits digital samples with sampling rate = 1.5 MHz calculated by applying the Shannon theory [3].

This digitized signal after the ADC shown in Fig.2(b) shall be fed to the DDLI as shown in Fig. 3. The O/P of the DDLI is compared with a selected threshold in order to make a decision about the presence of the target.

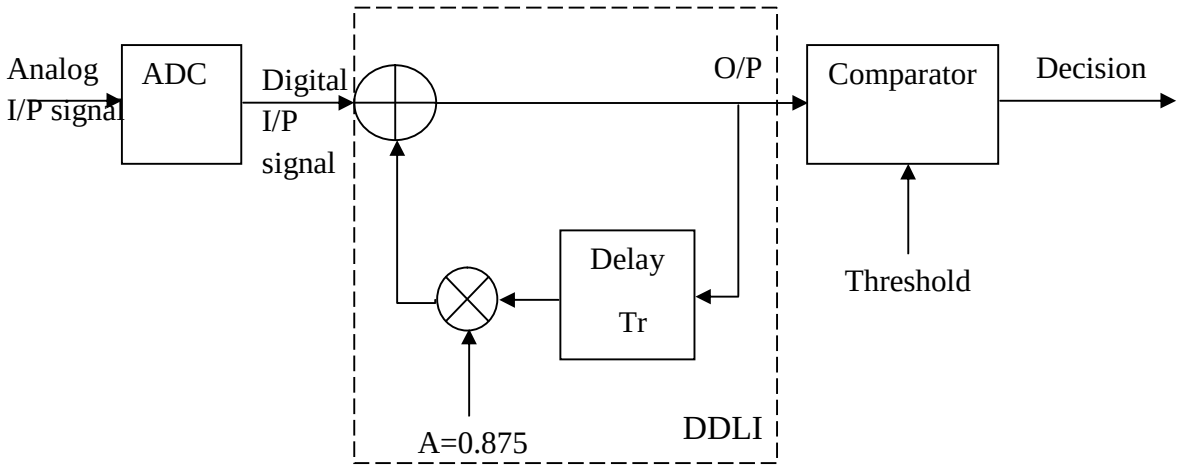


Fig. 3 The block diagram of the implemented recursive digital delay line

In the following sections, the design and implementation of the mentioned recursive DDLI using DSP and FPGA shall be introduced.

III. Design and Implementation of the DDLI using DSP

The TMS320C6416 DSK kit from Texas Instrument Company [4, 5] is used in the implementation process of the DDLI. The general block diagram of the implemented DDLI is shows Fig. 4. The O/P of the ADC is fed as I/P to the DSP kit. The DSP core contains three stages of the design, the timer, the DDLI and the comparator. These stages are designed using Code Composer Studio V.4. package.

The generation of the sampling rate is done by using hardware timer which is a peripheral in the C6416 DSP processor [4]. Its function is to count till certain value which is

predetermined and then gives an O/P pulse on a certain pin in the 6416 DSK (TOUT1 pin). This pulse is the clock pulse of the system (1.5MHz). This clock pulse is generated by dividing the DSP processor internal clock (125MHz) by (84) to get the slower clock pulse of 1.5 MHz

The generated clock pulse is used as I/P to the ADC as a start of conversion. It is used to establish the interrupt source of the DSP timer. The rising edge of this interrupt is used by the written program to fetch a new I/P sample. This sample shall be processed by the designed DDLI. The DDLI is achieved by using a circular buffer with size controlled by the period T_r (4050 sample).

The digitized video signal after the ADC is fed to the DSP kit through the I/P pins AED0 to AED5 (data input pins). This assigning is done via the written program to control the EMIFA (External Memory Interface A) of the DSP processor. Since the I/P signal of the used DSP processor is expressed as 32 bit integer number, anding the I/P 6 bits signal with 0x3F permits the use of only the least significant 6 bits in the EMIFA as input.

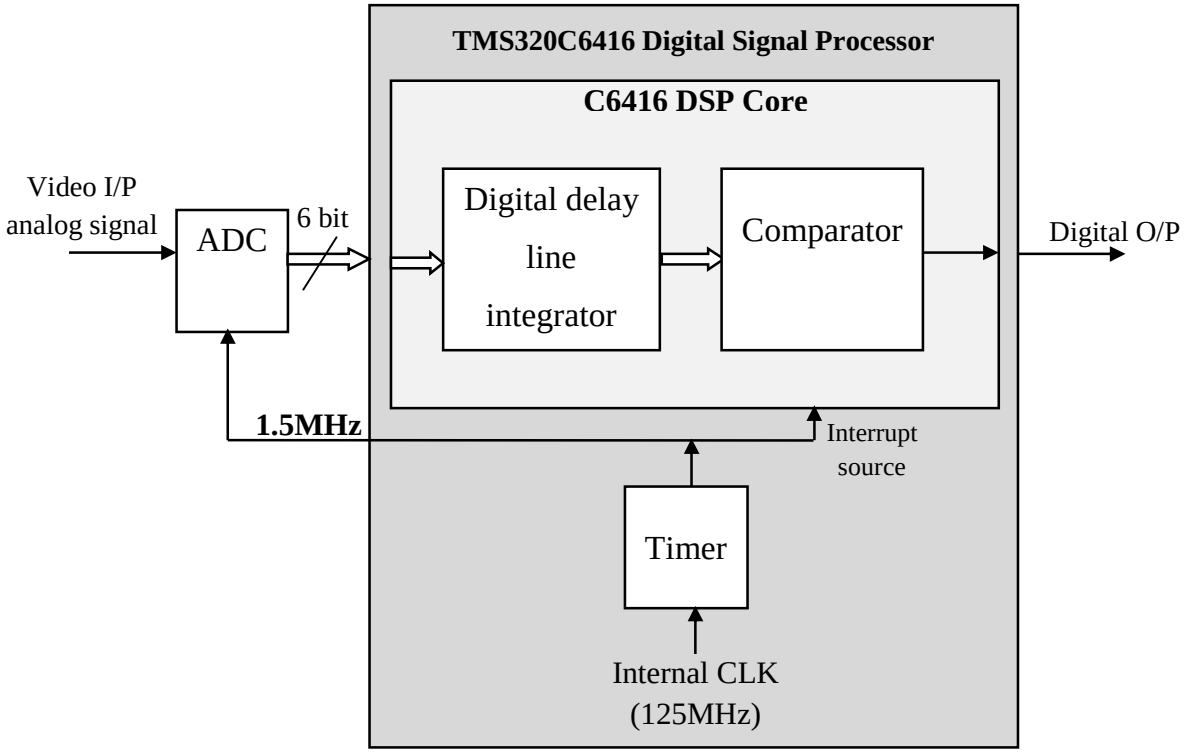


Fig. 4 The general block diagram of the designed DDLI using DSP

The I/P digital signal shall be stored in this buffer sample by sample respectively as the data comes in serial form. The delay is implemented by using the concept of circular buffer which uses two pointers (read pointer and write pointer) to read and write these samples in the buffer. For the first T_r, the I/P samples shall be written in the buffer using the write pointer with speed equal to the sampling rate.

A counter is designed to control the writing pointer of the buffer. The trigger pulse of the radar station is used as I/P to enable to the counter. The counter will start counting at the trigger and rest at the next trigger. This process is done to ensure that even if there is any change in T_r the system will work correctly.

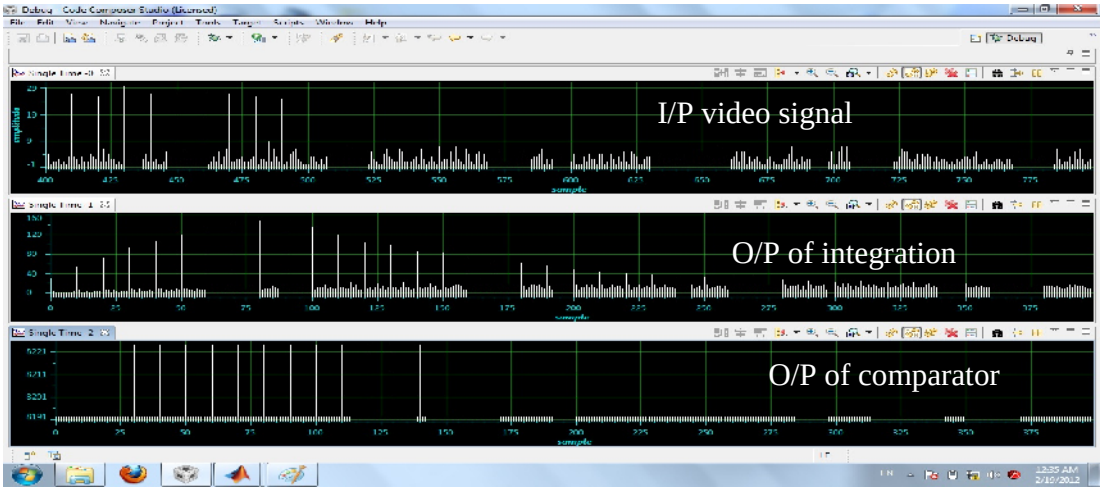
The read pointer using the processor speed reads the first stored sample from the buffer and multiplies it by the factor (0.875) and the result from this multiplication is summed with the first sample in the next T_r. The result of this operation is stored temporary in a temp value. The write pointer writes this temp value in the zero address of the buffer instead of the first sample of the previous pulse (feedback loop). The oldest element is over- written by the newest one.

The multiplication process is achieved by shifting left the 6 bit sample read from the buffer by one bit (dividing by 2), two bits (dividing by 4) and three bits (dividing by 8) respectively, the three shifting results are added. The result from this process corresponds to multiplying the input sample by (a = 0.875).

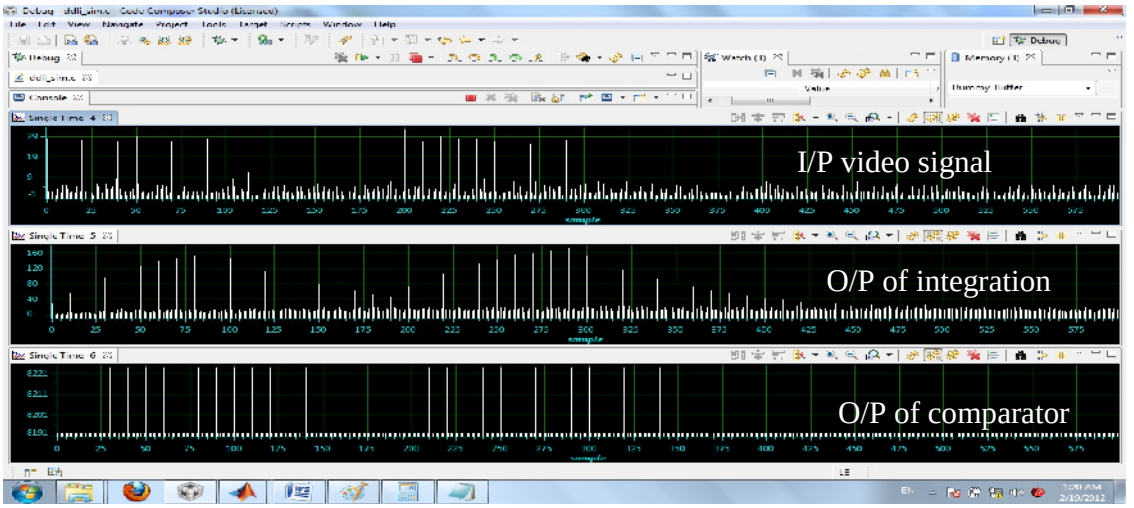
The O/P of the integration process is compared with a certain threshold to take a decision. The O/P of the comparator is logic one for target presence and logic zero for target absence. This O/P is assigned to one of the serial port pins that can be used as GPIO (general Input Output Pin) [6].

The system execution time using DSP in the implementation of the DDLI was 7.13 nsec and so the maximum sampling frequency is 140.25MHz

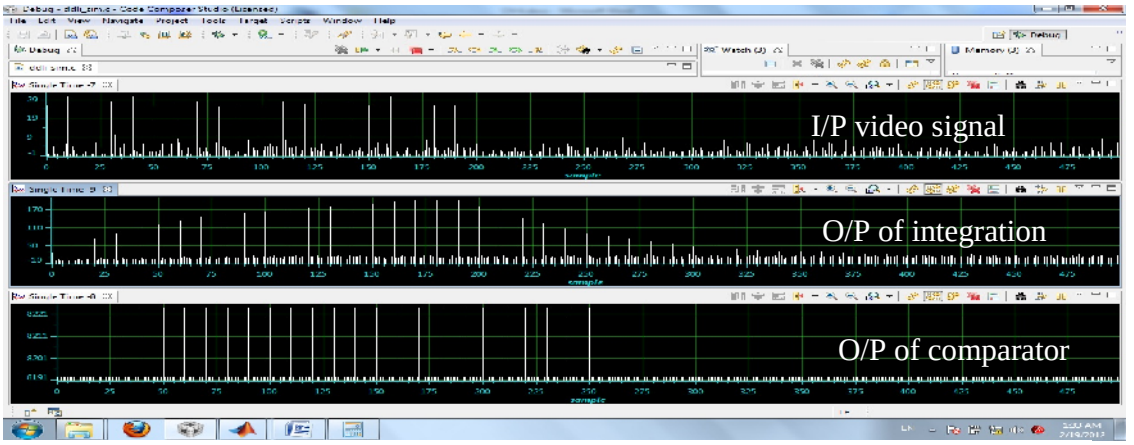
For the purpose of simulation, input video signal corrupted with noise with SNR=10dB for different target scenarios is simulated using Matlab package. This simulated video signal is used in the program for simulation. Results of this simulation are shown in **Error! Reference source not found.**



(a) simulation results of one target in one beam



(b) simulation results of two targets with one beam separation



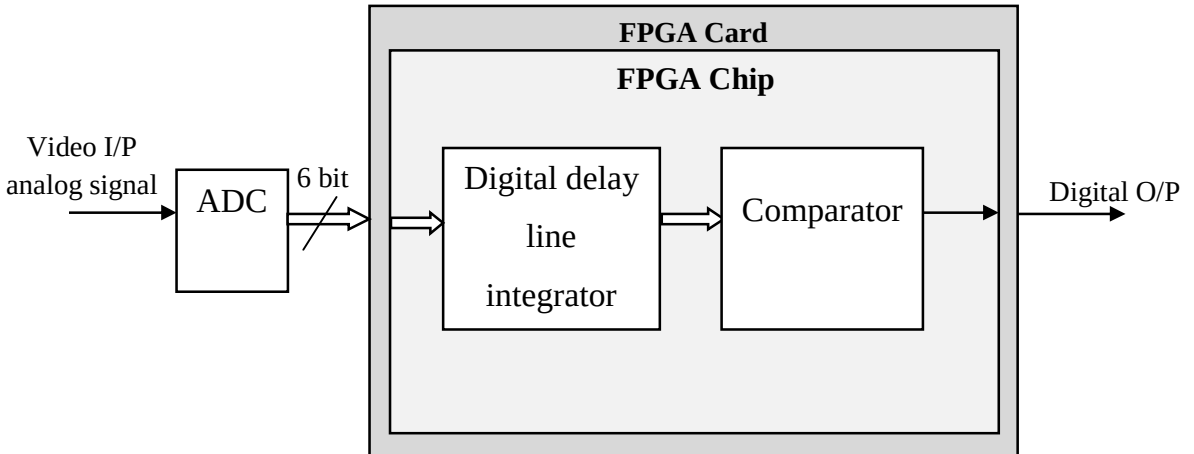
(c) simulation results of the two targets in two adjacent beam

Fig. 5 Simulation results for three target scenarios of the implemented DDLI using DSP

IV. Design and Implementation of the DDLI using FPGA

The DDLI is designed and implemented based on FPGA using the Xilinx package ISE 9.1i with the ModelSim 6.3 simulator .The design was downloaded on the Spartan 3-200k starter kit [7,8]. The general block diagram of the implemented DDLI is shown in Fig. 6

The implementation of the delay line is simply done with using the same idea as in DSP implementation. But instead of the buffer, FPGA uses a RAM to store and delay the data. The RAM width is determined by the integrated signal word length (12bit). The RAM depth is controlled by the period T_r (4050 sample). As in DSP a counter is designed to generate the address for the RAM.



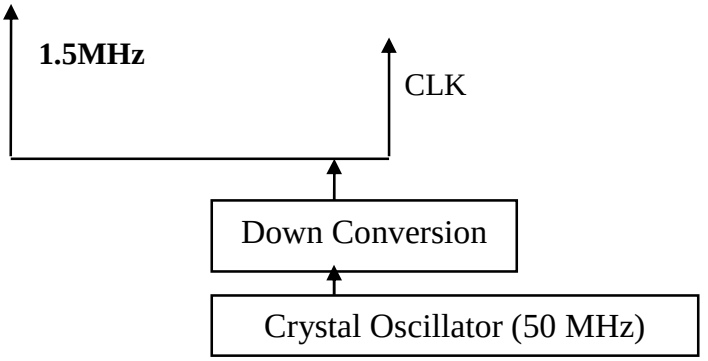
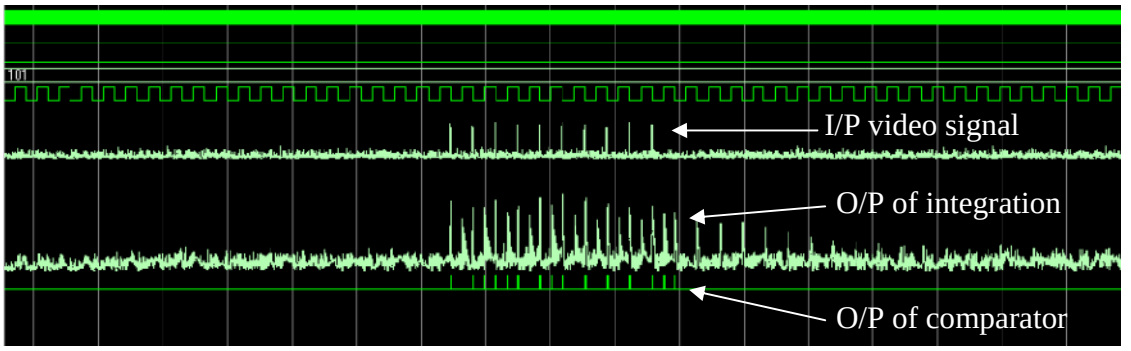


Fig. 6 The general block diagram of the designed DDLI using FPGA

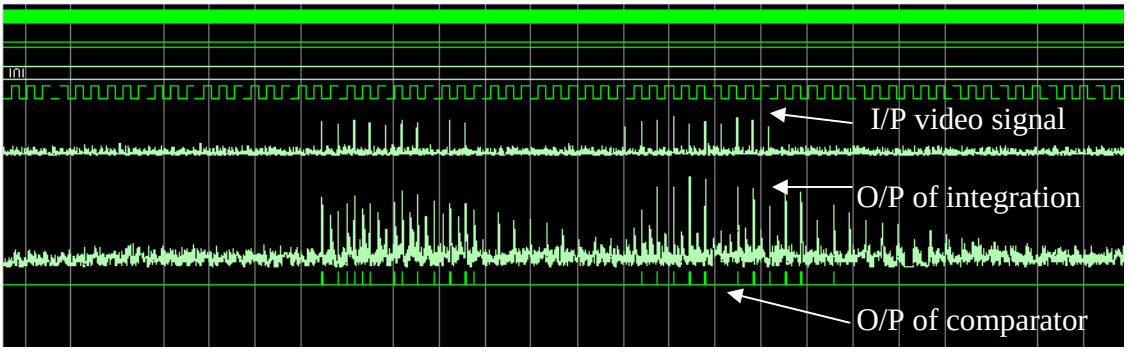
The generation of the sampling rate is achieved in FPGA by down conversion process. The on kit crystal oscillator (50 MHz) is divided by (32) to get the desired clock 1.5 MHz. This clock is used as I/P to the ADC as a start of conversion and as the designed system clock.

The minimum clock period for this design is found to be 14.377 nsec and the corresponding maximum sampling frequency is 70 MHz

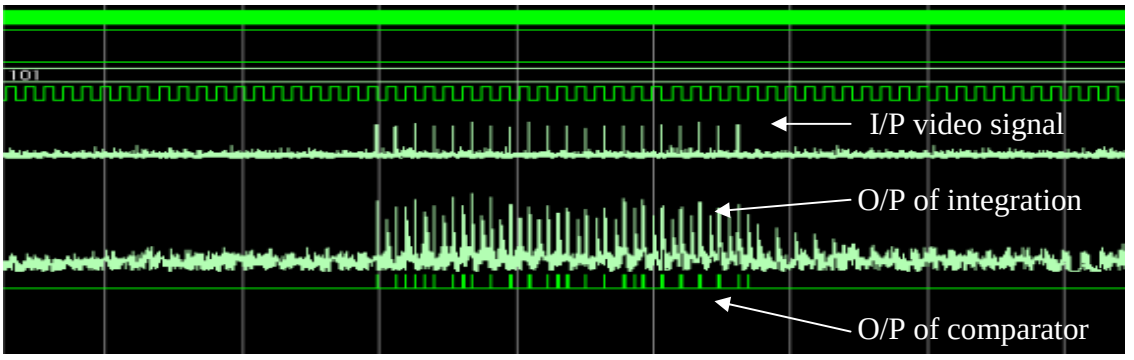
To simulate the performance of the implemented DDLI using FPGA, the same procedure which was used with the DSP design is used her. However, results of simulation using FPGA is shown in **Error! Reference source not found.** for different scenarios.



(a) simulation results of one target in one beam



(b) simulation results of two targets with one beam separation



(c) simulation results of the two targets in two adjacent beam

Fig. 7 simulation results for three target scenarios of the implemented DDLI using FPGA

V. Conclusion

The selection between DSP and FPGA platforms to design and implement radar signal processing circuits is a critical issue. Based on the proposed design and implementation (using DSP and FPGA) of the recursive DDLI, the DSP platform was the better choice. This is for the sake of sampling rate/speed, development time, conditional operation, and memory. From the experience achieved through the present paper, the main aspects for choosing between DSP and FPGA platforms can be summarized as shown in Table (1).

	FPGA	**DSP**
Sampling Rate	Higher	Few MHz
Data Rate	Higher	20-30 Mbyte/s
Conditional Operation	No	Yes
Floating Point Operation	No	Yes
Ready-Made Libraries	Yes	Yes
Cost Performance (MMAC)	High	Low
Power Consumption	Low	High
Design Reliability and Ease of Maintenance	Yes	No
Cost: Development Time, Time to market and risk	No	Yes
Flexibility	Yes	No
Re-configurability	Yes	No
Memory	No	Yes
Context Switching	Yes	No
Skills and Expertise of the designer	Equal	Equal

Table 1 General Comparison aspects in choosing DSP or FPGA

References

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[5] http://www.ti.com/

[6] Texas Instrument, "TMS320C6000 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide", Literature Number: SPRU580E, 2005

[7] http://www.xilinx.com

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