

**Military Technical College
Kobry El-Kobbah,
Cairo, Egypt**



**11th International Conference
on Electrical Engineering
ICEENG 2018**

Efficient GPS Signal Acquisition Based on Parallel FFT in FPGA

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ABSTRACT:

Acquisition in GPS system is crucial step to get the code phase in Pseudo Random Noise (PRN) in continuous tracking of the satellite. Fast Fourier Transform (FFT) in conventional GPS receivers usually is implemented in convolution algorithm in the acquisition process. In this paper, a parallel FFT algorithm is described that segments the fast Fourier transform algorithm into groups of identical parallel operations that can be performed concurrently and independently. The proposed algorithm is carried out using the LABVIEW FPGA module and those obtained from the GPS Signal simulation using LABVIEW verify the results. This process execution provides a superior performance in fast acquisition and determinism compared with conventional processors based software solutions.

KEYWORDS:

GPS , Signal acquisition , C/A code , PRN , FFT , Correlation , LABVIEW , FPGA

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NOMENCLATURE

GPS: Global Positioning System.
C/A code: Coarse Acquisition Code.
PRN: Pseudorandom Noise.
FFT: Fast Fourier Transform.
FPGA: Field Programmable Gate Arrays.
RF: Radio Frequency.
LFSR: Linear Feedback Shift Registers.

1. INTRODUCTION

The Global Positioning System (GPS) receiver in L-band is an embedded system programmed to find the location of the user position via solving the navigation equations besides finding its velocity and the accurate time [1,2]. The system constitute of thirty-two different satellites, each of which orbits the Earth approximately once every 12 hours. The orbits of the satellites have been set such that 6 satellites are available at every location on the earth. There are a set of different GPS carriers with data streams. The carrier and data stream employed in this work is the civilian-access signal, Coarse Acquisition (C/A). The (C/A) code is at the L1 band with carrier frequency 1575.42 MHz. Each data message contains a set of coarse satellite positioning parameters (almanac), an atmospheric correction model, and the satellite's orbital parameters (ephemeris).

Acquisition and tracking of GPS satellites are the main processes run in a GPS receiver. Software GPS receivers capture the RF modulated signals at L1 frequency, down-convert them to an intermediate frequency (IF), digitize them, and perform signal processing to extract the position information from the navigation message [3]. GPS receivers are considered as software defined radio (SDR), enable to have flexibility and low cost for modifying algorithms based on field programmable gate arrays (FPGA) and chips of digital signal processing[6,7].

The paper is structured as follows. In section 2, the Coarse Acquisition (C/A) is revised. A general architecture of the SDR GPS receiver is given in section 3. The three standard methods of GPS signal acquisition are discussed in Section 4. While, in section 5 the FFT algorithm is applied using the Cooley–Tukey algorithm with radix-2. Finally, section 6 explores the Implementation of Faster FFT and Finding the Correlation of GPS Signal Using LABVIEW and CompactRIO and conclusion of this work is given in section 7.

2. COARSE ACQUISITION (C/A) CODE

C/A code is a pseudorandom sequence of 0s and 1s based on Gold codes and is unique for every satellite. The C/A code operates at a frequency of 1.023 MHz. Sets of two Gold codes with different phase tapings are used to produce unique C/A code for every satellite. The algorithm of C/A code for a particular satellite is developed to deliver the identification number of the GPS satellite, such that a unique code for each satellite is generated. The spread spectrum and code modulation of L1 GPS carrier is shown in Fig. 1 [5].

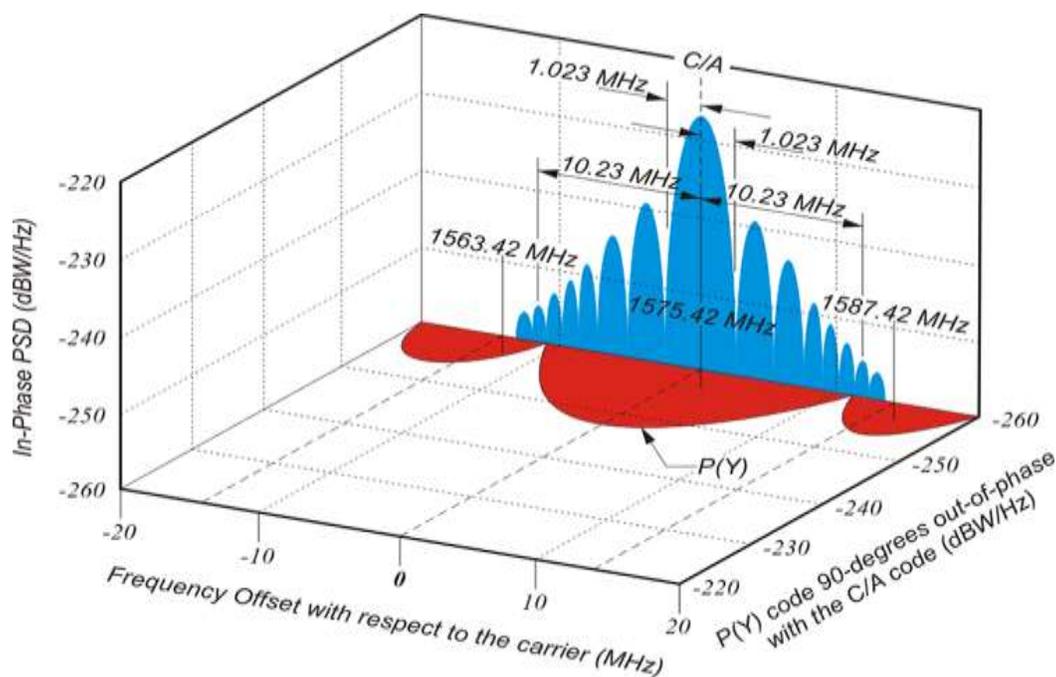


Fig. 1: Spread Spectrum and Code Modulation of L1 GPS Carrier [5]

As shown in Fig.2, two 10-bit linear feedback shift registers (LFSRs). G1 and G2 generate maximum-length pseudorandom codes with a length of $2^{10} - 1 = 1023$ bits. A modulo-2 adder is used to generate the C/A code, which uses the outputs from G1 and G2 as inputs. Initially, both G1 and G2 are all set to 1's since the all-zero state is illegal. The G1 and G2 LFSR's feedback taps are defined by the generator polynomials [4]:

$$G1 = 1 + y^3 + y^{10} \tag{1}$$

$$G2 = 1 + y^2 + y^3 + y^6 + y^8 + y^9 + y^{10} \tag{2}$$

$$Gi = G1(10) \oplus G2(P1) \oplus G2(P2) \tag{3}$$

Where G_i : Gold code sequence for i th satellite vehicle (SV_i),

P1,P2: Signal tap values predefined for i th satellite

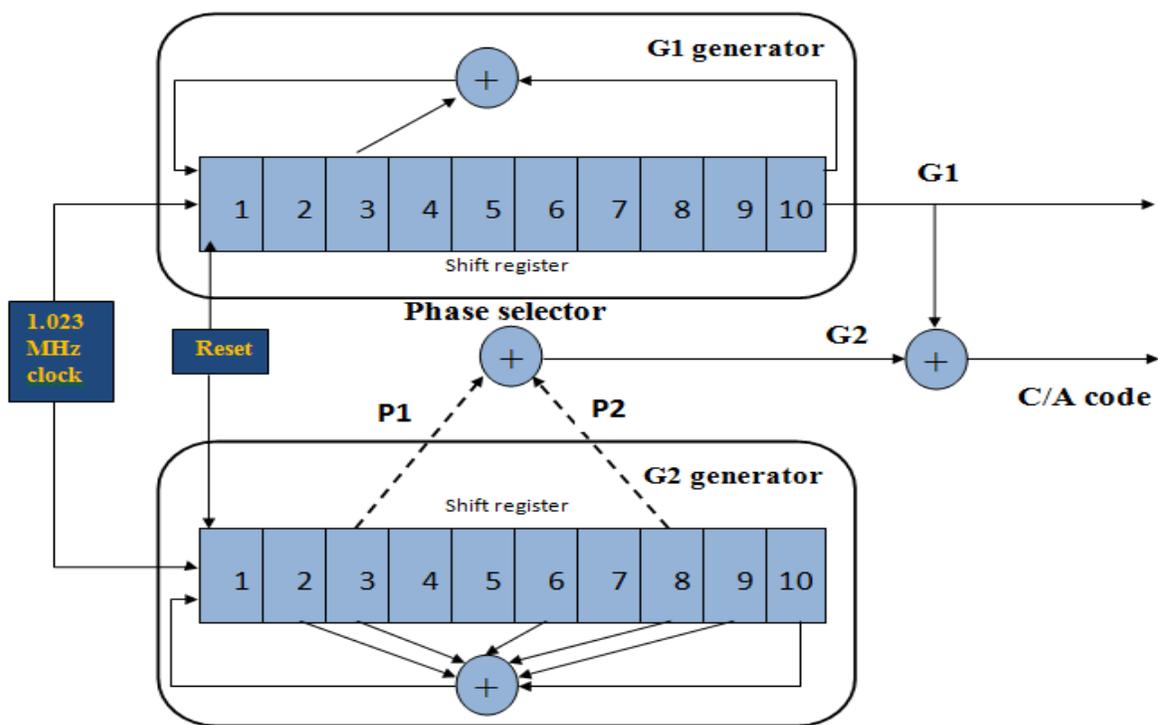


Fig. 2: C/A Code Generator

The satellite identification is determined by the two output positions of the G2 generator. There are 37 unique output positions, of which 32 are utilized for the C/A codes of 37 satellites. As

only 32 satellites are in orbit, the other 5 outputs are reserved for other applications such as ground transmission [6].

3. General block diagram for software defined GPS receiver

A general architecture of the SDR GPS receiver is shown in Fig.3 where, the antenna receives the GPS signals from visible satellites (at least 4 satellites), where these signals travel about 20,000 km until reach to the receiver with power $\approx 10^{-16}$ watts.

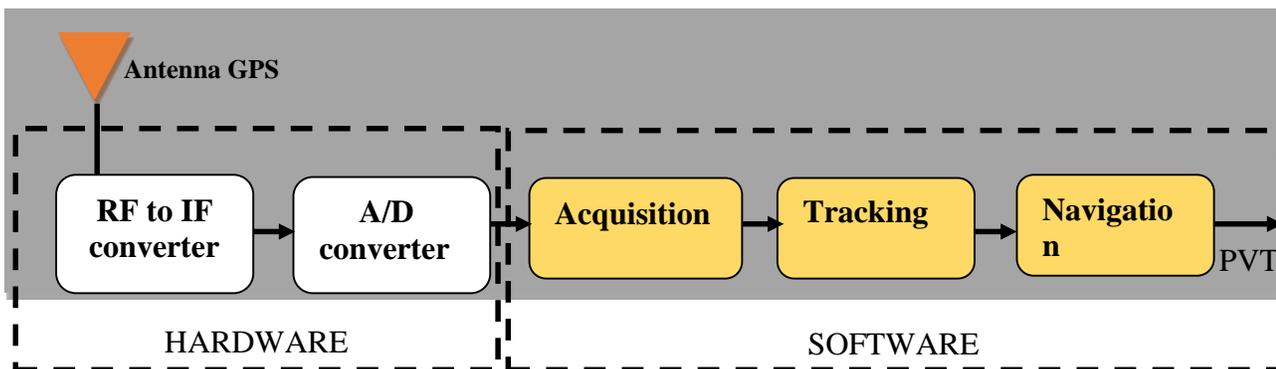


Fig. 3: block diagram of SDR GPS receiver

- In front end stage(Hardware) the receiver must remove interference ,amplify the power of the signal and convert the radio frequency(RF) to intermediate frequency (IF) by local oscillator and mixer as a converter to improve the performance of the receiver ,then convert this analog (IF) signal to digital (IF) signal.
- The following stages is called the processing of the signal (Software Implementation) that based on a channelized structure, the receiver must distinguish which satellites are presently visible,The acquisition stage gives rough estimation for the parameters of the signal and get the code phase and Doppler frequency (results from the movement between the satellite and the receiver),These estimated parameters refined by the two blocks of tracking stage(code tracking and carrier tracking) .
- The output of the tracking stage help the receiver to estimates the pseudorange of the tracked satellites after extract the navigation data , then compute the positions of same satellites at transmit time in order to solve the navigation equation by least square

method to get the position of the receiver (latitude and longitude) , the velocity and the time of the receiver.

4. GPS SIGNAL ACQUISITION

Acquisition technique is finding the beginning of the C/A code that uses to despread the spectrum. When the spectrum is despread, the output becomes a continuous wave signal and we can find the carrier frequency for it. The beginning of the C/A code and the carrier frequency are the factors delivered to the tracking stage[3].

4.1 The three standard methods of acquisition [6]

- **Serial Search Acquisition**, This method is one of the first methods used in acquisition in code division multiple access (CDMA) system, the algorithm is based on multiplication of locally generated PRN code sequences and locally generated carrier signals.

- **Parallel Frequency Space Search Acquisition**, This procedure is Very time Consuming, and the technique utilizes the Fourier transform to perform a transformation from the time domain to frequency domain.

- **Parallel Code Phase Search Acquisition**
 - Parallelizes the code space dimension.
 - Multiply the incoming signal with a locally generated sine and cosine.
 - Perform a Fourier transform of this signal combining I and Q into a complex signal.
 - Perform a Fourier transform and a complex conjugate of the locally generated C/A code.
 - Multiply the signals in the frequency domain.
 - Perform an inverse Fourier transform to obtain the output in the time domain.

4.2 Correlation Based on FFT

Mathematically, Correlation is the close cousin of convolution. The correlation between two continuous functions $g(t)$ and $h(t)$, which is denoted $\text{Corr}(g, h)$ [8], and is a function of time lag

t. The correlation will be large at some value of (t) if the first function (g) is a close copy of the second (h) but lags it in time by t, i.e., if the first function is shifted to the right of the second.

- The correlations using the FFT as follows:

The discrete correlation of two sampled functions g_k and h_k , each periodic with period N , is defined by

$$Corr(g, h)_j = \sum_{k=0}^{N-1} g_{j+k} h_k \quad (4)$$

The *discrete correlation theorem* says that this discrete correlation of two real functions g and h is one member of the discrete Fourier transform pair

$$Corr(g, h)_j \iff G_k H_k^* \quad (5)$$

Where G_k and H_k are the discrete Fourier transforms of g_j and h_j , and the asterisk denotes complex conjugation.

4.3FFT-based Parallel Search Acquisition

The main function of acquisition is to identify the available satellites in the received data and then find the code phase by correlating the incoming signal with the locally-generated C/A code and finding the carrier frequency, including the Doppler shift. This is done by correlating the incoming signal with the receiver generated signal [3]. If the two signals match we get a very high correlation peak. This peak value is compared within a certain threshold value, if it is greater, the satellite is said to be acquired. The well-defined acquisition method built in software GPS receivers is the FFT-based parallel search method as shown in Figure 4.

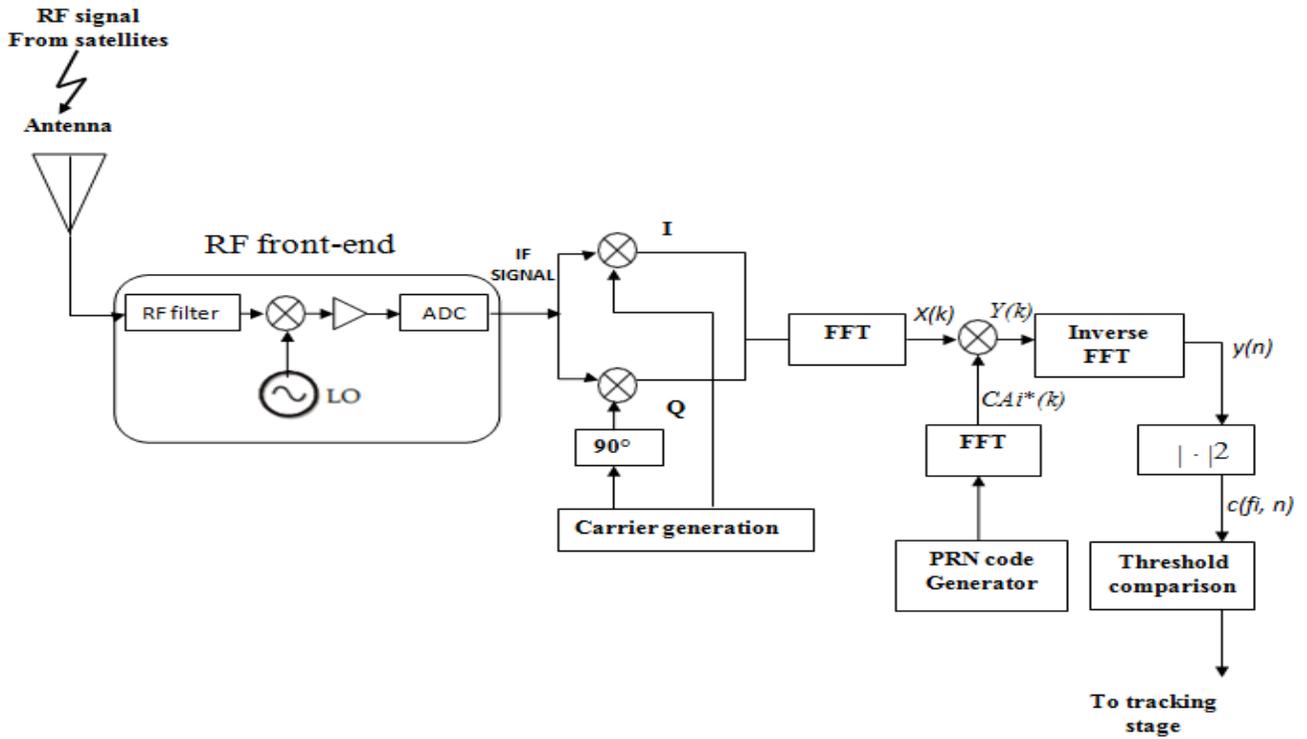


Fig. 4: FFT-based acquisition algorithm.

The complex form of the input signal I and Q signals are [4]:

$$x(n) = I(n) + jQ(n) \tag{6}$$

After combining the two and taking its FFT as in (7), it is multiplied with the complex conjugate FFT, denoted by *, for the *i*th satellite to be searched

$$X(k) = FFT[x(n)] \tag{7}$$

$$CA_i(k) = FFT[ca_i(n)] \tag{8}$$

$$Y(k) = X(k) CA_i^*(k) \tag{9}$$

The IFFT of the result as in (10) is squared, summed up to non-coherent integration period and compared with a pre-defined threshold value.

$$y(n) = IFFT[Y(k)] \tag{10}$$

$$c(f_i, n) = [y(n)]^2 \tag{11}$$

Where f_i is the locally generated carrier and n is the number of samples,
 If the correlation is above this threshold, the satellite is said to be acquired. The code phase is the value of phase for which the correlation has a peak value.

5. FFT Algorithm

This algorithm has length of the input sequence, N , can be represented as a power of 2 i.e., $N = 2^m$, Radix-2 algorithm [9-10]. This means that the number of complex additions and multiplications gets reduced to $N(N+6)/2$ and $N^2/2$ just by using the divide-and-conquer approach. When we also begin to use the symmetry and periodicity property of the twiddle factor, it can be shown that the number of complex additions and multiplications can be reduced to $N \log_2 N$ and $(N/2) \log_2 N$ respectively. Hence, from a $O(N^2)$ algorithm, the computational complexity has been reduced to $O(N \log N)$. The entire process is divided into $\log_2 N$ stages and in each stage $N/2$ two-point DFTs are performed. The computation involving each pair of data is called a butterfly. Radix-2 algorithm can be implemented as Decimation- in-time ($M=N/2$ and $L=2$) or Decimation- in- frequency ($M=2$ and $L=N/2$) algorithms. Fig.5 below gives the decimation-in- frequency form of the Radix-2 algorithm for an input sequence of length, $N=8$. Fig.6 below gives the decimation-in-time form of the same. The parallel composition of this algorithm is shown in Fig. 7.

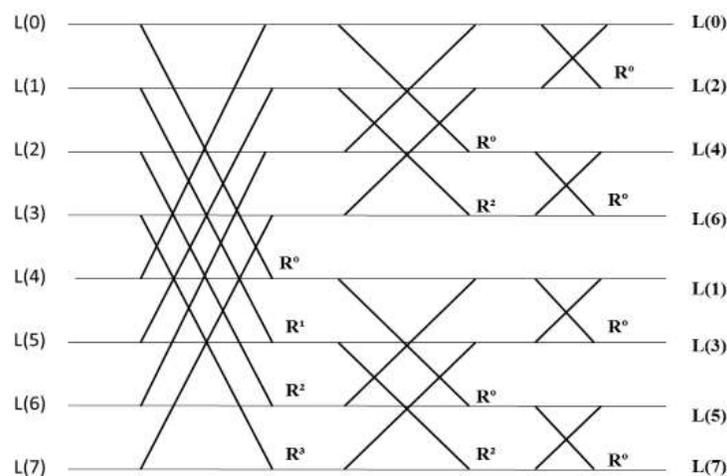


Fig.5: 8-point Radix-2FFT: Decimation in frequency form

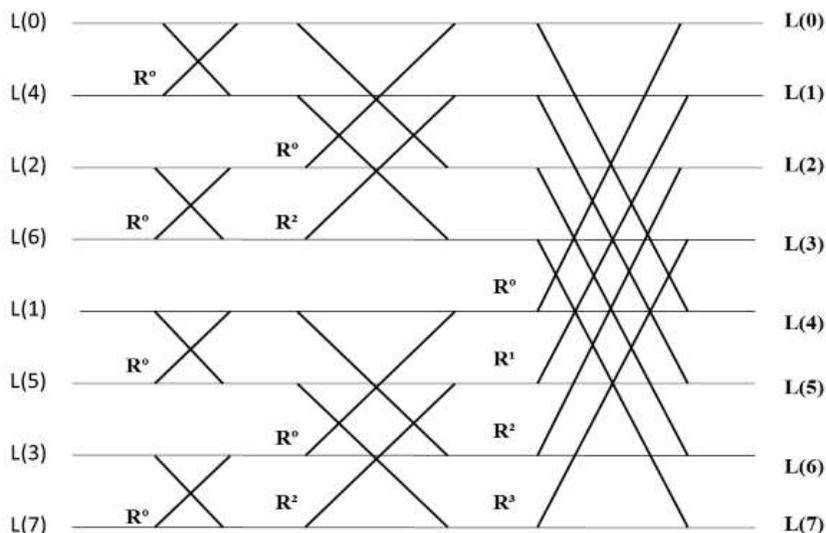


Fig.6: 8-point Radix-2FFT: Decimation in time form

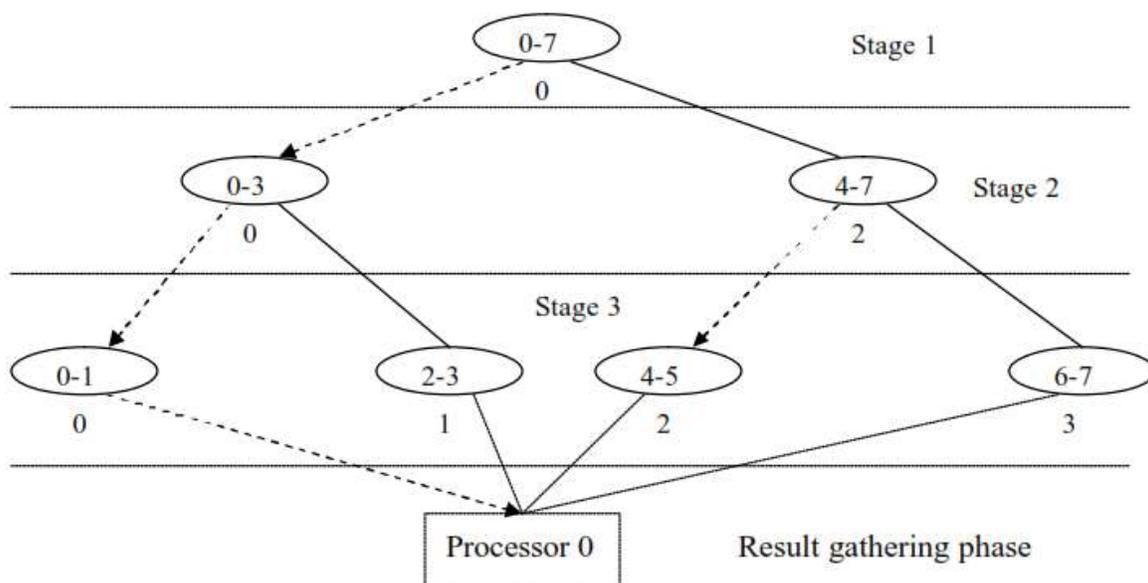


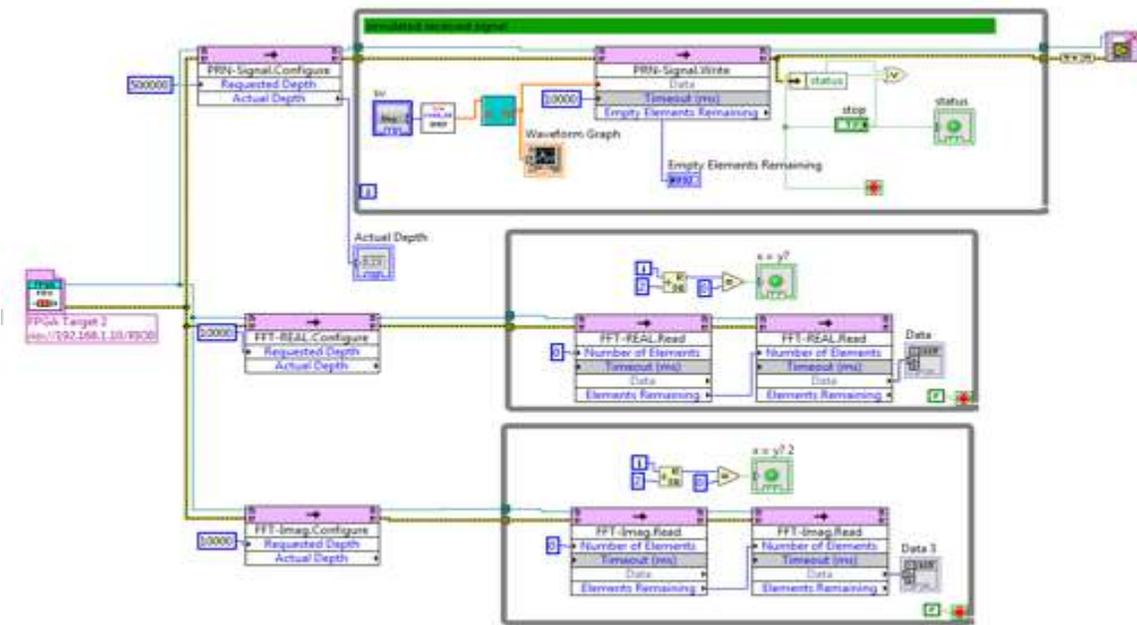
Fig. 7:Parallel composition for 8-point Radix-2 FFT in Decimation in frequency form On a 4 processor system [9]

6. Implementation of Faster FFT and Finding the Correlation of GPS Signal Using LABVIEW and CompactRIO

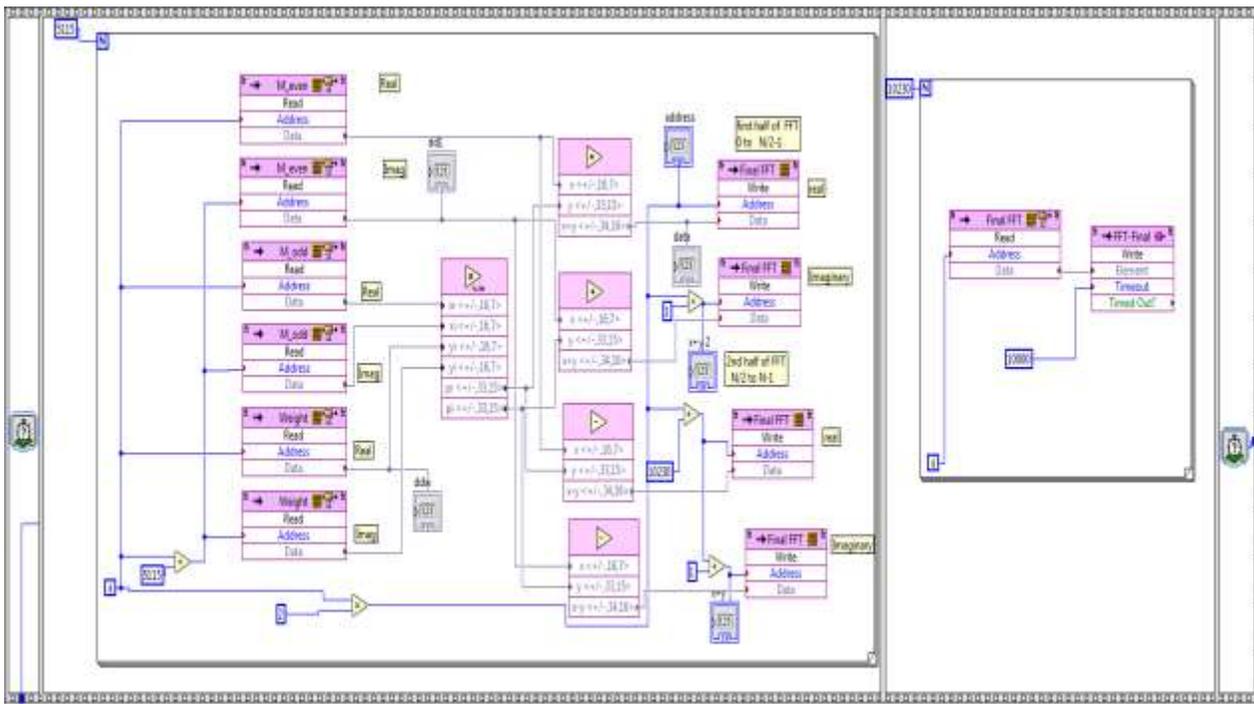
The LABVIEW real time software architecture is modular, where each module has a specific task such as I/O operations, analysis, monitoring, network communication and logging [11]. The proposed implementation has twoparts: HOST control and FFT code in FPGA mode. The CRIO-9014 Controller, 400 MHz PowerPC, 2 GB Storage, connected to an 8-slot chassis ni-9104. Fig.8 shows the FPGA VI for finding the FFT of a real-time signal and storing its value in memory. DMA-FIFO is used to store the data as even and odd samples and then find the FFT of each sampled data. Finally applying, the Cooley–Tukey algorithm [13], and then the stored data is transferred to the HOST. Direct implementation of the FFT algorithm without decimation is shown in Fig. 9

A comparison between the proposed implementation with samples decimation and direct implementation is given in table. 1. The comparison explore the execution time of applying Cooley–Tukey algorithm with radix-2 is much smaller than direct implementation of FFT approach in the expenses of using larger hardware FPGA gates and memory.

The GPS receiver essentially shifts the code that it has in its memory until it matches up with the one it received from the satellite. This is done by using the autocorrelation function based on the FFT of the received signal and the time shifted replica in the receiver. When the two codes match up, there will be a correlation spike, and from this, the receiver knows the clock offset from the number of chips it shifted the replica code by. Fig.10 shows two examples of the output of two autocorrelation processes. The top graph is what happens when we take the autocorrelation function of two different PRN numbers (PRN 3 with PRN 10). The lower shows the output of the autocorrelation processes of the sum of PRN 3 plus noise with PRN 3 shifted 350 chips.



(a)



(b)

Fig.8: The VI of the proposed implementation in LABVIEW a) Host part. b) FPGA part.

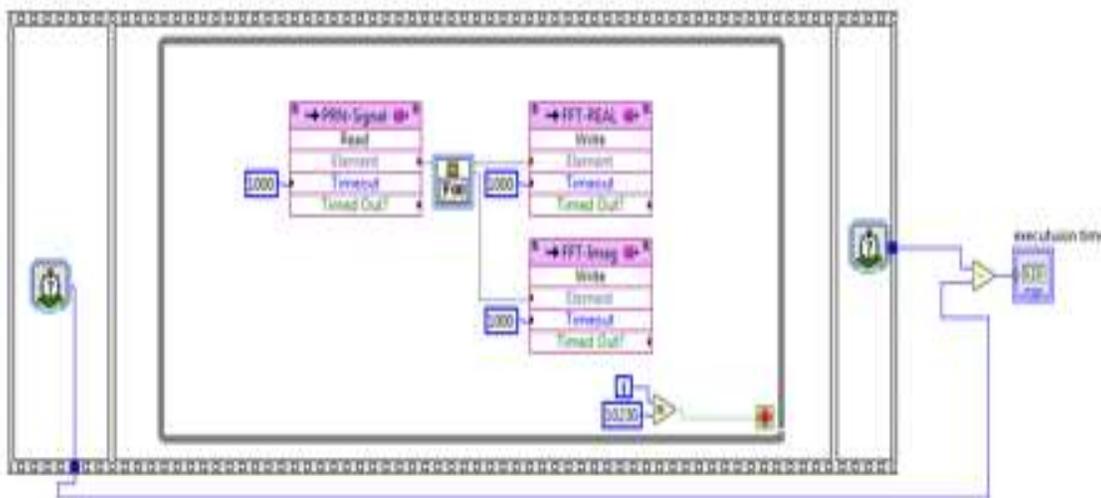
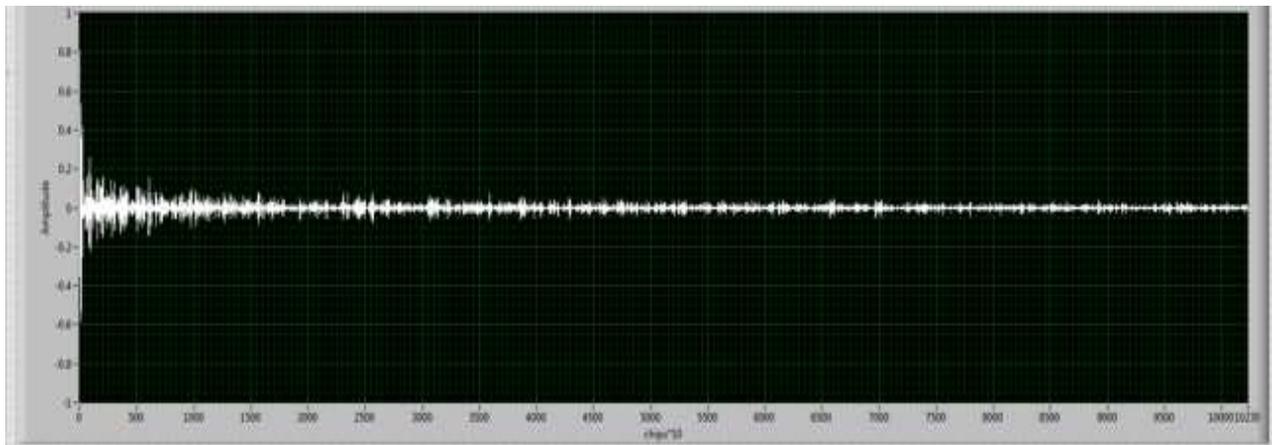


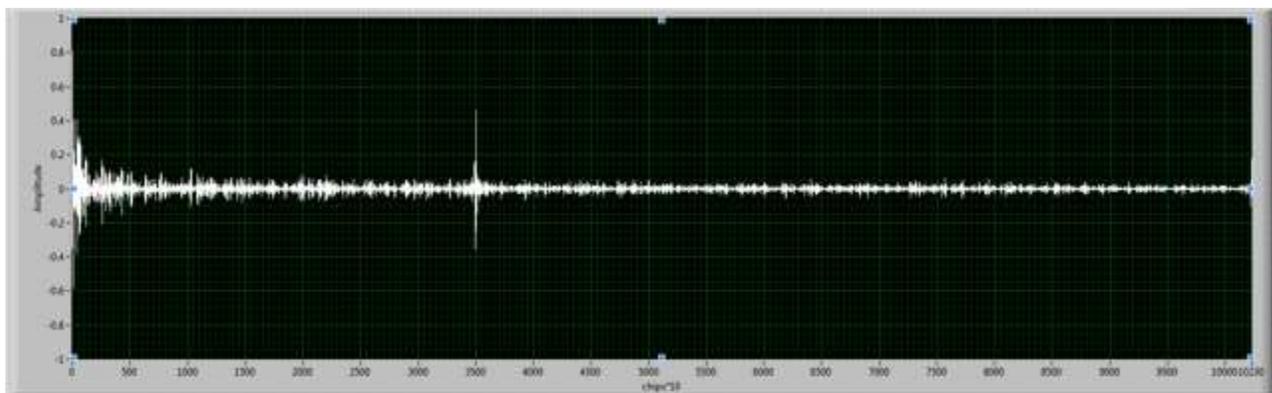
Fig.9 Direct implementation of FFT without Decimation.

Table-1 Comparison between the proposed implementation of FFT of GPS-signal and direct implementation.

	With decimation	Without decimation
Total Slices	Total Slices: 61.8% (8850 out of 14336)	Total Slices: 21.2% (3034 out of 14336)
Slice Registers	Slice Registers: 28.7% (8219 out of 28672)	Slice Registers: 9.8% (2808 out of 28672)
Slice LUTs	Slice LUTs: 45.1% (12941 out of 28672)	Slice LUTs: 15.6% (4463 out of 28672)
Block RAMs	Block RAMs: 24.9% (24 out of 96)	Block RAMs: 8.3% (8 out of 96)
Execution Time (mSec) (40 MHz Onboard Clock: 40.00 MHz (43.94 MHz maximum))	5.77077	19.572005



(a)



(b)

Fig.10 a) Autocorrelation of the sum of PRN 3 plus noise with PRN 10
 b) Autocorrelation of the sum of PRN 3 plus noise with PRN 3 shifted 350 chips

7- CONCLUSION

This paper devoted to the current challenges for developing a real-time base-band block processor for a GPS receiver based on FPGA Technology. The higher processing speed of GPS block is the main objective of this work. A fast and simple-to-implement acquisition algorithm based on averaging-correlation method was verified. The algorithm was implemented using acquisition-driven-correlators architecture for block processing and was mapped to an FPGA. Using the DMA-FIFO guarantees reduction in latency in data monitoring on the host and no data is missed with improved throughput. The realised architecture satisfies real-time processing and tracking accuracy that makes it a crucial key in designing a GPS receiver for real-time applications.

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