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A Fully Differential Chopper Circuit in 130nm CMOS for Noise Minimization in Sensor Applications

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Abstract: For sensor applications, the bandwidth of interest is generally a few hertz. In this bandwidth, offset and 1/f noise are the dominant sources of error. Chopping technique is an efficient approach to decrease the 1/f noise and low-frequency offset of CMOS amplifiers; thus, in this paper, a proposed chopper circuit to tackle these problems is presented. The chopper circuit is designed using complementary CMOS switches that are optimized to achieve symmetric linear resistance in the range of input signal. The proposed circuit has a low ON resistance that only varies within 8% of its value for a rail to rail input. To validate its operation, it is used to build up a fully differential chopper stabilized CMOS amplifier powered at 1V. The resulting circuit achieves a thermal noise floor of 10 nV/√Hz and reduces the input referred noise corner frequency from 1-kHz to300mHz.

Keywords: Input referred noise, offset, charge injection, chopper circuit.

1. Introduction

Integrated circuit (IC) design has increasingly focused on lower power consumption, lower voltage and minimum size, contributing to the development of many devices[1],[2] . Reducing the area diminishes the size and weight of electronic devices, making it more user-friendly. Low voltage operation and low power dissipation are essential to increase battery lifetime in electronic devices; however, they correspond to poor noise immunity, especially when the device includes analog circuitry. An important source of noise encountered in low-voltage, low-power devices is flicker (1/f) noise, which is associated with the circuitry of an operational amplifier (op amp)[3].Chopper stabilized CMOS differential instrumentation amplifier is adopted to reduce 1/f noise [4].

Chopper circuits suffer from a very troublesome problem, namely charge injection[5],[6]. Furthermore, variations of the chopper switches ON resistance within the chopped signal range present another challenge in chopper circuit design. Various chopper circuits have been proposed in the literature in an attempt to overcome these problems[7], [8].

This paper tackles this issue, where a chopper circuit is proposed & optimized for optimum performance. The proposed circuit has a low ON resistance that varies only within a small percentage of its nominal value for a rail to rail input. The paper is organized as follows: section 2 gives a brief introduction about chopper stabilization as a method of noise reduction within analog circuits and the design of different chopper circuits. Section 3 outlines the

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design and the optimization of the proposed chopper circuit, also the layout and post layout Simulation of the proposed chopper circuit. Application of the designed chopper circuit on fully differential amplifier is outlined in section 4. Finally section 5 concludes the paper.

2. Chopper Stabilization Technique

2.1 Principle of Operation

Chopping is a modulation technique that is employed to reduce the effects of op-amp imperfections including noise and dc offset voltage. Figure 1shows the principle of chopper amplifier together with its ideal waveforms in time domain. The input voltage V_{in} first passes through a chopper circuit which derived by clock at frequency f_{ch}, so this signal is modulated at f_{ch}. Next, the modulated signal is amplified together with its own input offset. The second chopper circuit demodulates the amplified input signal back to DC, and at the same time modulates the offset to the odd harmonics of f_{ch}, where they are filtered out by a low-pass filter (LPF). This results in an amplified input signal without offset as shown in figure 1.

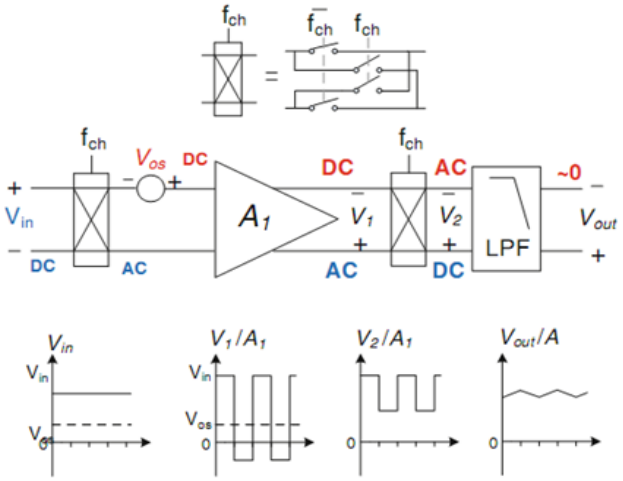

Fig. 1: Chopping principle in time domain[9]

The other Low-frequency errors, such as 1/f noise will be modulated and filtered out along with offset and this can be seen in figure2, which shows the chopping action in the frequency domain. The input signal is firstly modulated by the chopping signal with frequency f_{ch} and shifted to odd harmonics of the chopping frequency, as shown in figure2(b)and represented by the following equations.

Let the input signal be denoted by $V_{in}(t)$ and the chopper frequency be denoted as f_{ch} then the chopped signal is given by,

$$V_{in_{ch}}(t) = V_{in}(t)\cos(2\pi f_{ch}t) \tag{1}$$

If V_n denotes the flicker noise of the amplifier, and V_{os} denotes the amplifier's input-referred offset. The input of the amplifier is given by,

$$V_{input} = V_{in_{ch}}(t) + V_n(t) + V_{os} \tag{2}$$

Let the gain of the amplifier be A. The output of the chopper amplifier is given by

$$V_{out} = A.V_{input}.\cos(2\pi f_{ch}t) \tag{3}$$

$$V_{out} = A.[V_{in_{ch}}(t) + V_n(t) + V_{os}].\cos(2\pi f_{ch}t) \tag{4}$$

$$\begin{aligned} V_{out} &= \frac{A}{2}V_{in}(t) + \frac{A}{2}V_{in}(t).\cos(4\pi f_{ch}t) \\ &+ A.[V_n(t) + V_{os}].\cos(2\pi f_{ch}t) \end{aligned} \tag{5}$$

where, V_{os} and V_n denote the dc offset and noise of the amplifier, respectively. After amplification, the modulated input signal is demodulated to the even harmonics, and the noise and DC offset before the amplifier is just modulated once and shifted to the odd harmonics of the chopping frequency, as shown in figure 2 (c).The low pass filterfilters out the noise and dc offset, leaving base-band input signal without any distortion as shown in figure 2 (d).The cut-off frequency of chopper amplifiers should be higher than the chopping frequency to prevent attenuation of input signal which be converted to f_{ch}.

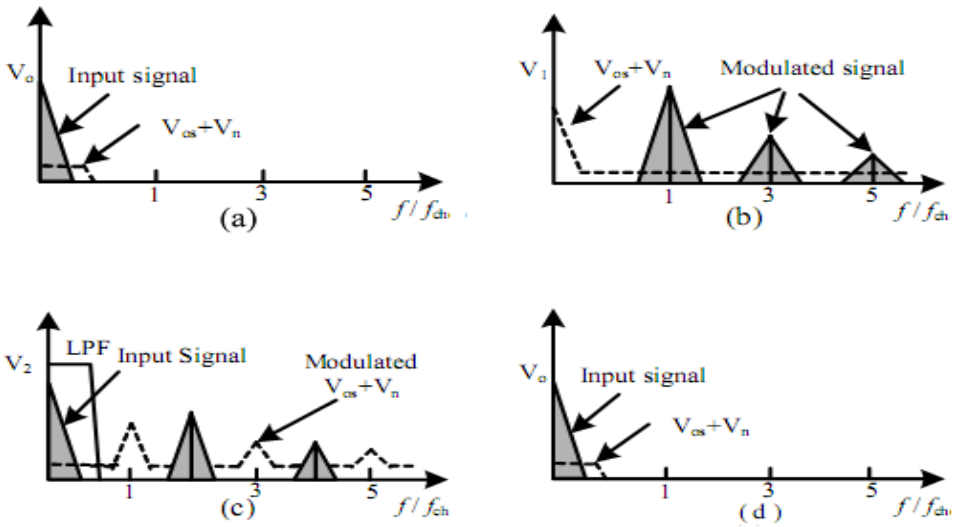

Fig. 2: Chopping principle in frequency domain

2.2 Chopper Circuit Using NMOS Switches

The conventional approach of using a single NMOS transistor in designing a chopper circuit is shown in figure 3. Unfortunately, this simple structure suffers from some problems; charge injection and clock feed-through are two main sources of offset problems [5]. Offset can totally impair the operation of such a circuit especially in low voltage operation. Another well-known drawback of such a circuit is the inevitable dependence of its operation on the magnitude of the input signal which leads to large variation in its ON resistance as depicted in figure 4.This nonlinear variation in the ON resistance results in the nonlinearity of output signal.

2.3 Chopper Circuit Using CMOS Switches

To reduce the effect of charge injection, chopper circuit using complementary CMOS switches, as shown in figure 5, is used. The complementary CMOS switch consists of an nMOS transistor and a pMOS transistor in parallel with gates controlled by complementary signals. This structure acts as a voltage-controlled resistor connecting the input and the

output[2]. Furthermore, with careful design, this structure can provide a linear on-resistance within the full-range of the input swing[10].

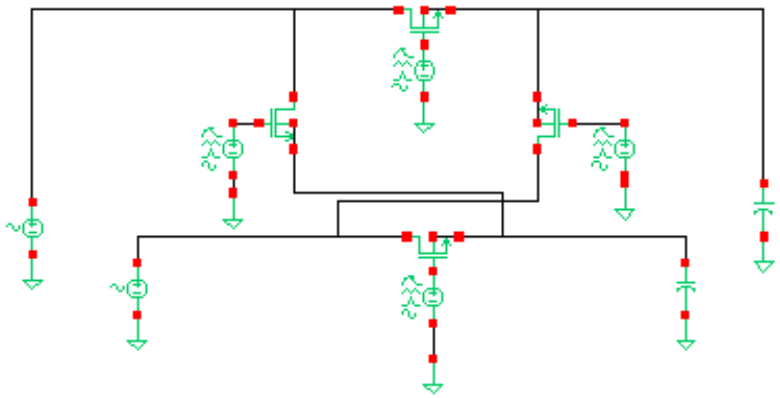

Fig.3: Conventional chopper circuit using NMOS switches

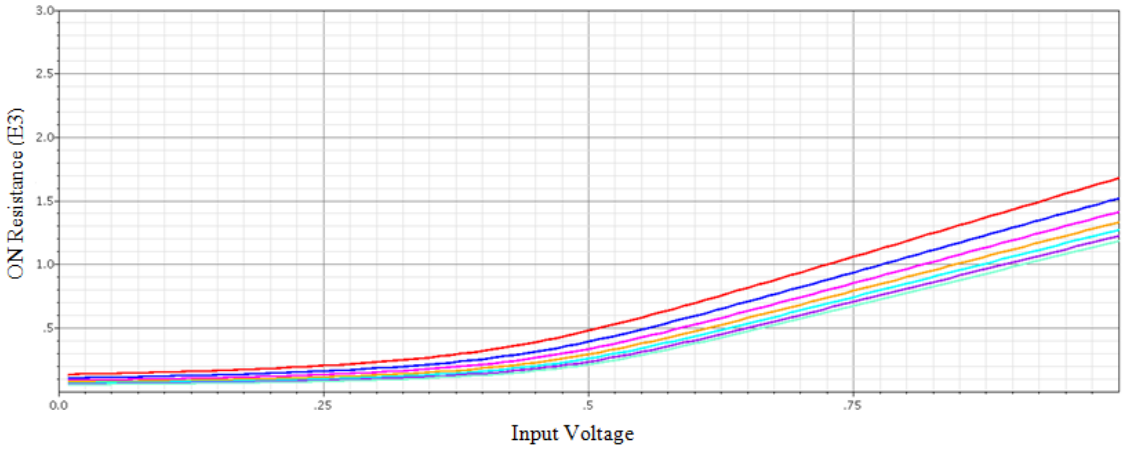

Fig. 4: ON resistance for NMOS switches versus the input voltage (W_n varies from 4-10µm)

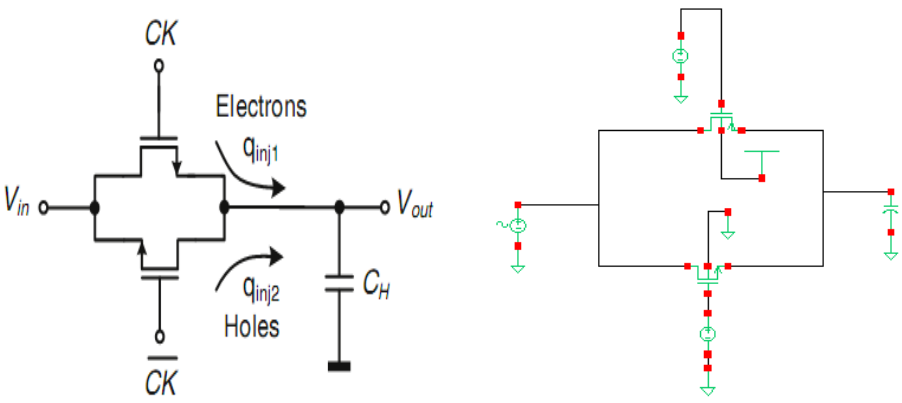

Fig.5: Complementary CMOS switch

3. Proposed Design

3.1 Optimized CMOS Chopper Circuit

To obtain a near constant ON resistance within the input signal range, the sizing of the complementary switches needs to be optimized. Accordingly, this is applied to the circuit depicted in figure 5. Assuming a rail-to-rail input voltage extending from 0 to 1-V, the input voltage to the chopper circuit is swept within this range. The chopper switch ON resistance is plotted for different values of the W/L ratios of the PMOS and NMOS transistors as shown in figure 6. The simulation shows that when the W_p / W_n ratio is 14/4, the effective ON-resistance across the full range of the input voltage is approximately symmetrical with minimum variation.

Unfortunately, this optimized design still suffers from clock feed-through. This problem can be reduced through the use of dummy switches, or differential structure [10]. In the following section, a proposed solutionthat alleviates this problem is presented.

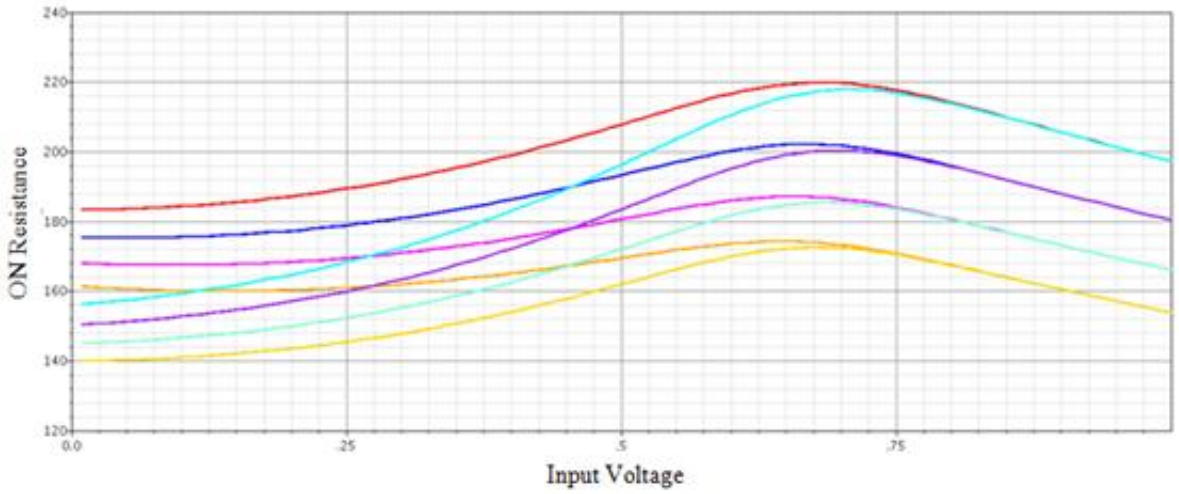

Fig.6: ON resistance curve of improved complementary switch versus the input voltage (W_n varies from 3 - 4µm and W_p varies from 11-14µm)

3.2 Fully Differential CMOS Chopper Circuit

In order to suppress the effect of charge injection and clock feed-through, the complementary CMOS switches are used in fully differential structure as shown in figure 7 to best compensate for this effect.

3.3 Layout of the Proposed Chopper Circuit

Figure 8 shows the layout of the chopper circuit with an overall on chip area of 140µm^2. Calibre interactive tool from Mentor Graphics is used to perform verification of the circuit including Design Rule Check (DRC), Layout versus Schematic (LVS), and Parasitic Extract (PEX).

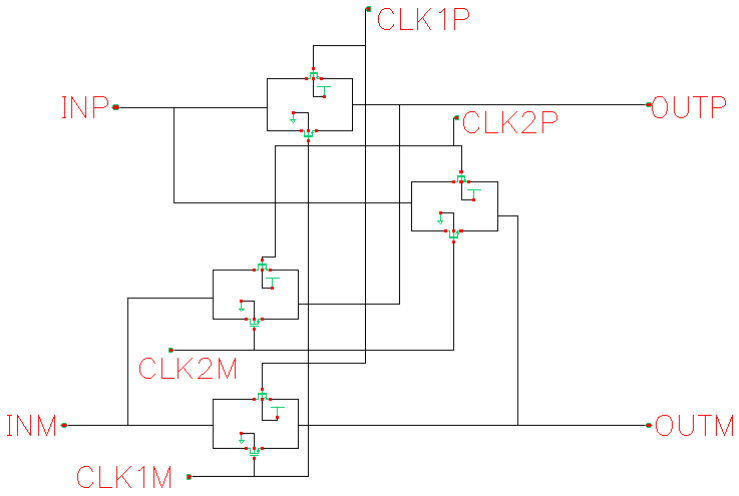

Fig. 7: Complete Circuit Diagram of Fully differential Chopper circuit

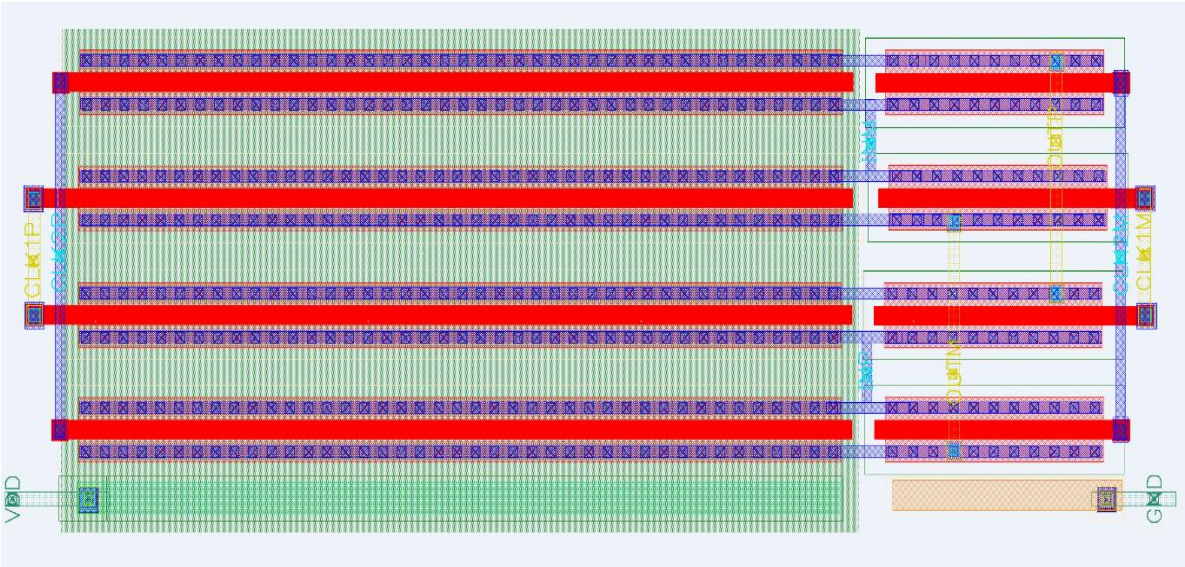

Fig. 8: Layout of Chopper Circuit

3.4 Simulation Results

In conventional SPICE-like simulators, a linear time-invariant model of the circuit is constructed before simulation, which linearizes the circuit at the quiescent operating point (the DC solution). These conventional analyses cannot handle frequency translation because they analyze a linear time-invariant representation of the circuit. The chopper circuit has frequency translation and is not linear time-invariant. So, SPICE-like simulators cannot be used to simulate the chopper amplifier. Spectre RF simulator extends the traditional time-domain algorithms to handle these frequency translation circuits[11].

In this paper, we employ the Spectre RF simulator to design/analyse the chopper amplifier circuit. The circuit of the proposed chopper amplifier is implemented using TSMC 0.13µm CMOS technology. The supply voltage is 1Vand the chopping frequency is 10 KHz. Post layout simulation is performed after parasitic extraction and the simulation results are shown in figure 9, where the input and output signals from the simulation of the chopper/modulator circuit in transient time domain are shown.

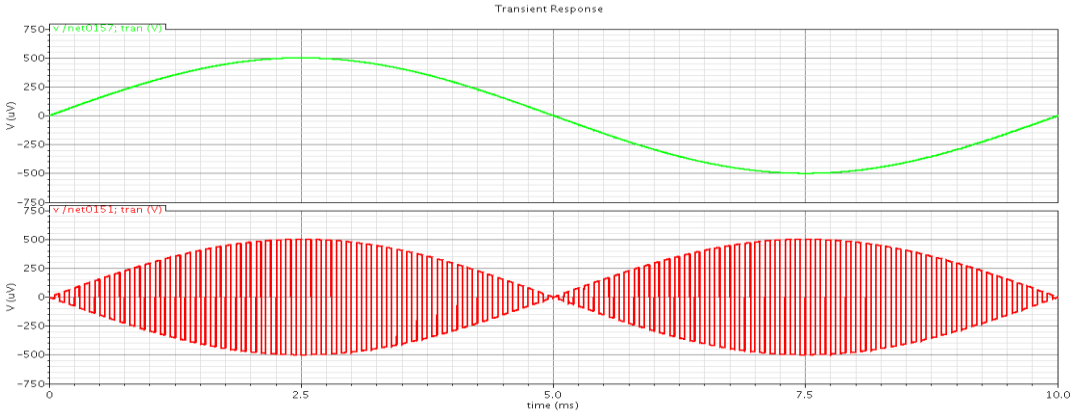

Fig. 9: Input and output signals from chopper circuit

4. Application Circuit: Fully Differential Op-Amp

To verify the operation of the proposed chopper circuit, a fully differential amplifier as in [12] and depicted in figure10 is used. The block diagram for the complete chopper instrumentation amplifier circuit is shown in figure 11.

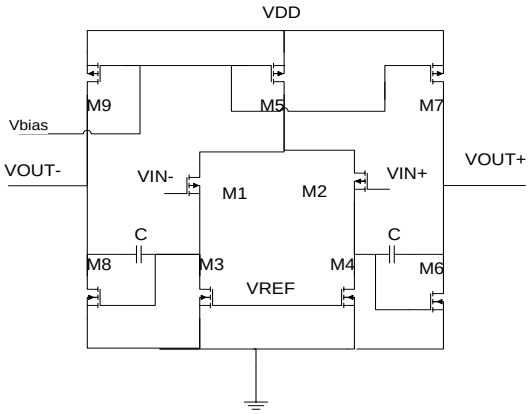

Fig. 10 Fully differential OP-AMP

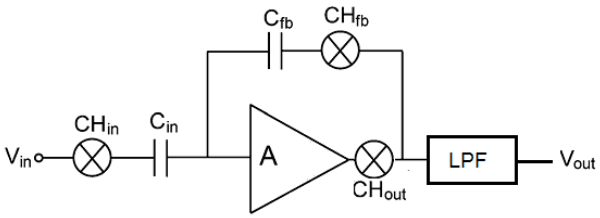

Fig. 11 Simplified block diagram of a complete amplifier

Figure 12 shows the input-referred noise density of the designed instrumentation amplifier circuit using the proposed differential chopper circuit. The upper line of the figure presents an input-referred noise of 160 nV/√Hz and corner frequency around 1kHz without using the chopper circuit, while the lower line has 10 nV/√Hz input noise and corner frequency around 300mHz when using the chopping method.

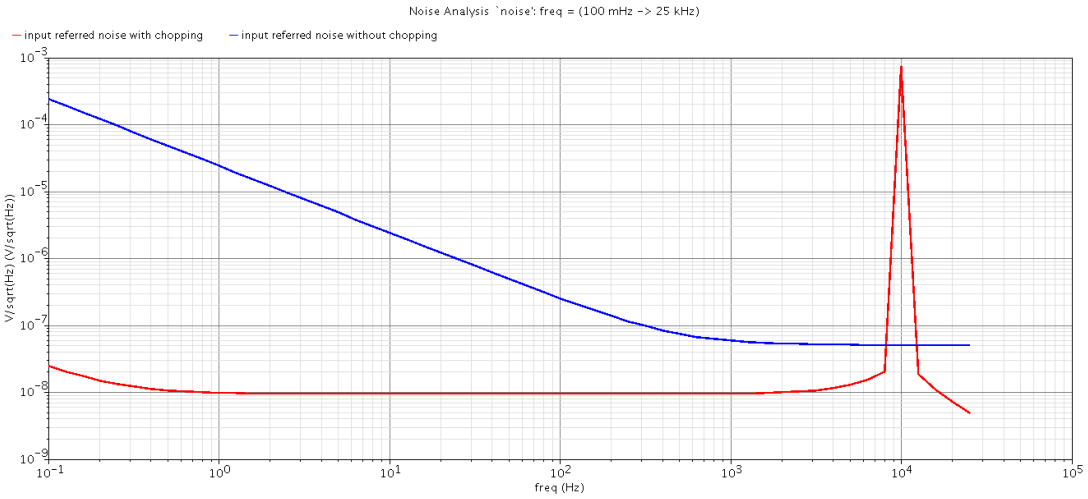

Fig. 12: Input referred noise without and with chopping

5. Conclusion

In this paper, a fully differential chopper circuit is designed using 130 nm CMOS technology using complementary CMOS switches that are optimized to achieve symmetric linear resistance for rail-to-rail input signal. The proposed differential structure achieves a small ON resistance with a relative variation smaller than 8% for a rail-to-rail input change. The designed circuit is successfully used within a chopper stabilized instrumentation amplifier. The resulting structure achieves thermal noise floor of 10 nV/√Hz with the corner frequency of the input referred noise reduced from 1-kHz to 300-mHz.

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