

Design of an Analog Front-End (AFE) for Photoplethysmography (PPG) Acquisition System

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ABSTRACT

This paper implies a low power photoplethysmography (PPG) sensor circuit. PPG sensors are widely used in modern healthcare products for monitoring cardiovascular information. The PPG Signal can reveal diverse conditions, such as respiratory and cardiac arrest, systemic inflammatory response syndrome, renal insufficiency, cardiac insufficiency, systolic arterial pressure, among others. The low-power Analog Front-End (AFE) of the PPG sensor is designed in 0.18 μm CMOS process. The AFE amplifies the weak photocurrent from the photodiode (PD) and converts it to a strong voltage at the output by the means of Transimpedance Amplifier (TIA). To decrease the power consumption, the circuits are designed in subthreshold region; so, the total biasing current of the AFE is a few microwatts. The TIA core, consisting of a self-biased two-stage Miller OTA, operates with a Bandgap Reference (BGR) to manage supply voltage fluctuations. A voltage-to-current converter with a BGR ensures a stable and accurate current output, minimizing dependence on temperature and supply variations. Pseudo-resistance provides the large resistance needed for high TIA gain while maintaining a small chip area. DC offset, which affects TIA operation and amplification, is addressed. An IDAC controlling circuit is used for DC cancellation, enhancing the amplifier's dynamic range by keeping the AC signal clear at the output.

1. Introduction:

Heart diseases are considered as a major public health problem, since they are the leading cause of death worldwide, especially in populations of large urban centres. According to data from the World Health Organization, 17.3 million people died in 2012 as victims of this type of disease. The estimate is that, by 2030, this number will be 23.6 million. Mortality rates are steadily rising. Therefore, it is important to adopt preventive measures and control various risk factors, such as hypertension, diabetes and smoking [1-6]. Photoplethysmography (PPG) is one on the most popular technologies in the last decade for monitoring of the physiological conditions of a patient because it is a non-invasive method [7-20]. PPG has been largely applied to personal portable devices and pulse oximetry due to its convenience and capacity to perform continuous readings. The PPG signal can provide information about both the cardiovascular and respiratory systems [21-26].

The PPG technique relies on Beer–Lambert's law, which states that light intensity decreases exponentially in an absorbent medium and is wavelength-dependent. The law relates emitted light intensity to incident light,

considering absorption, solution concentration, and light path. Higher LED luminosity increases transmitted and reflected light. Individual physiological differences, such as skin tone, fat layer thickness, and radial artery rigidity, significantly affect the plethysmographic wave's morphology and amplitude [27-32].

Photoplethysmography sensors measure the amount of infrared light absorbed or reflected by blood. Volume changes are caused by pressure changes in blood vessels, which occur throughout the cardiac cycle. PPG is based on the properties of light scattering caused by glucose in blood. The increase in glucose decreases the misalignment of the light beam penetrating the tissue, because the refractive index is reduced by its presence [33-36].

A PPG signal has several components including volumetric changes in arterial blood which is associated with cardiac activity and variations in venous blood volume which modulates the PPG signal. A DC component showing the tissues' optical property and subtle energy changes in the body [37-40]. Some major factors affecting the recordings from the PPG are the site of measurement and the contact force between the site and the sensor. Blood flow variations mostly occur in the arteries and not in the veins [41-44].

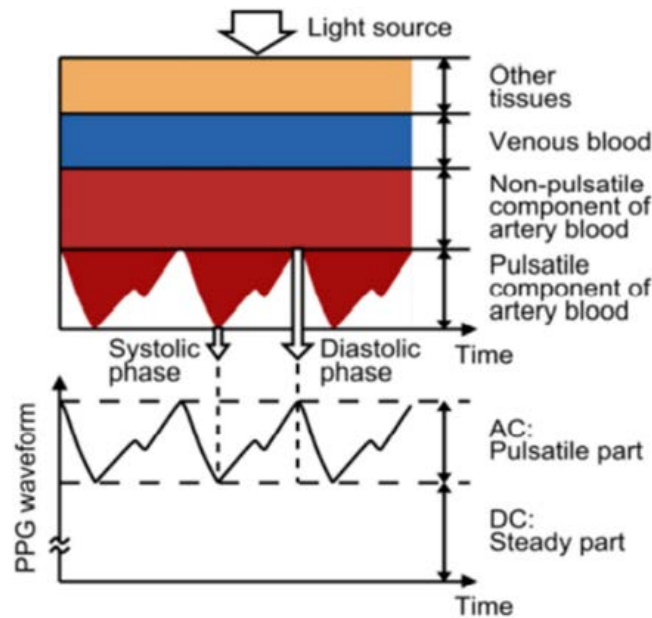


Fig. 1. PPG Signal Attenuation through the skin [7]

PPG shows the blood flow changes as a waveform with the help of a bar or a graph. The waveform has an alternating current (AC) component and a direct current (DC) component, see Fig. 1.

2. System Design

First the photodiode receives the reflected light from human tissue after it has been modulated in accordance with the blood behavior inside the peripheral vessels. The received signal has two components; The AC component is the desired one, corresponds to variations in blood volume in synchronization with the heartbeat. The DC component arises from the optical signals reflected or transmitted by the tissues and is determined by the tissue structure. The basic frequency of the AC component varies with the heart rate and is superimposed on the DC baseline. Our desired output is the PPG signal, AC part, filtered and amplified.

The Signal is then applied to a Transimpedance Amplifier which converts the weak input photocurrent to amplified output voltage. The TIA core is made of a Self-biased Two-stage Miller OTA and is operated with a Bandgap Reference (BGR) to deal with the supply voltage fluctuations. A voltage to current converter circuit is used with a Bandgap Reference (BGR) to ensure a stable and accurate current output that is less dependent on temperature variations and supply variations. A pseudo-Resistance is used to provide a large value of resistance that is required for obtaining the large TIA gain while keeping a small chip area. The DC offset affects the operation of the TIA and the amplification level, so it is taken into consideration. IDAC Controlling circuit is used for DC cancellation to keep the AC signal acquiring at the output, which enlarges the amplifier's dynamic range.

2.1 Transimpedance Amplifier TIA

The main function of a transimpedance amplifier is to convert a current input signal into a proportional voltage output signal. In other words, it measures the current flowing through its input and produces a voltage output that is directly proportional to that input current, see Fig. 2. The TIA has a configuration where the signal input is applied to the inverting input of an operational amplifier (op-amp). A feedback resistor R_f is connected between the output of the op-amp and its inverting input (virtual ground). This resistor plays a crucial role in converting the current input to a voltage output. When a current I_{in} flows into the inverting input of the op-amp, according to the virtual ground concept in op-amp circuits, the same current I_{in} flows through the feedback resistor R_f . The op-amp amplifies the voltage drop across the feedback resistor to generate the output voltage V_{out} . It maintains the virtual ground at its inverting input to ensure the current I_{in} through R_f .

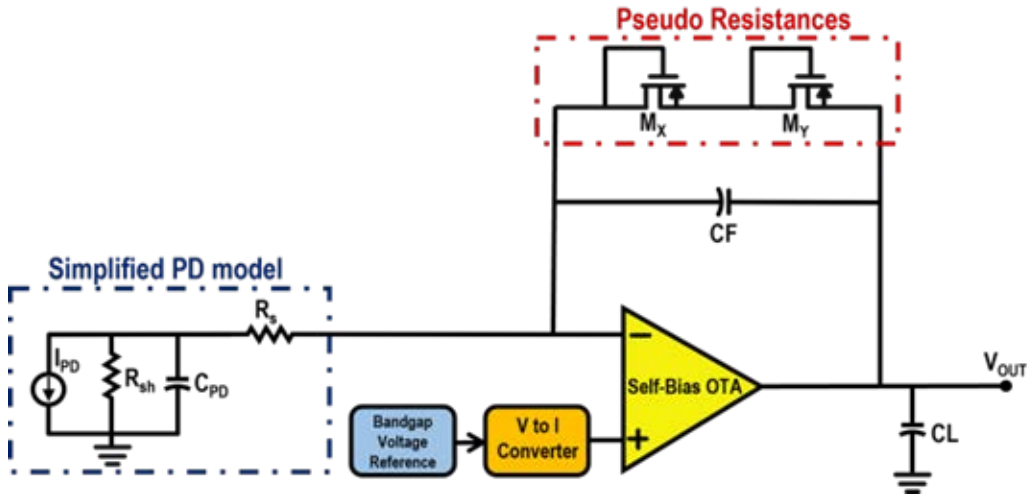


Fig. 2 Transimpedance Amplifier Schematic.

$$f_{3dB} = \frac{1}{2 \pi R_f C_f} \quad (1)$$

In this work, Transimpedance Amplifier (TIA) has achieved gain levels about 143.542dB and Bandwidth of 6.874 kHz, the supply voltage is 1.8V in 0.18 μm CMOS process. The current TIA is 1nA and the output voltage is 1.49V. The Total Harmonic Distortion (THD) of the output signal is 133.29u% at input current 1 nA, 311.03u % at 2nA, 1.53m % at 3nA, 101.21m % at 4nA, 7.13 % at 5nA, 12.52 % at 6nA, 16.50% at 7nA, 19.55 % at 8nA, 21.97 % at 9nA and 23.94 % at 10nA.

2.2 Pseudo Resistance

Instead of using a physical resistor, pseudo resistance in a TIA can be implemented using active components like MOSFETs or BJTs. Effective resistance can be controlled electronically, allowing for dynamic adjustment of the amplifier gain, see Fig. 3. The gate voltage of the MOSFET controls effective resistance, enabling dynamic adjustment of the TIA's gain. The pseudo resistance that is used in the design is TSCM-I with a value of and with $(W)L=2/1$.

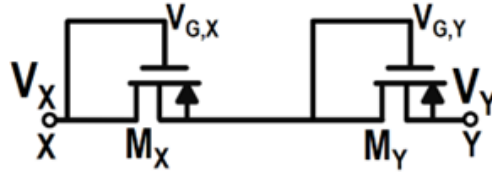


Fig. 3 Pseudo Resistance

$$R_{YX} = \frac{\partial v_{YX}}{\partial i_{YX}} \quad (2)$$

2.3 Photodiode Modeling

Typically, photodiodes are modeled using a current source that represents the photocurrent generated by the device. Using a current source to model the photocurrent generated by the photodiode simplifies the modeling approach by abstracting the internal mechanisms of the photodiode if the photodiode generates a current directly proportional to the incident light intensity as previously discussed.

For a typical device, the model we choose for our design includes a light-dependent current source in parallel with a large shunt resistor (hundreds of MΩ) and a shunt capacitor that can range from less than 50 pF for small devices to more than 5000 pF for very large devices, see Fig. 4 and Fig. 5.

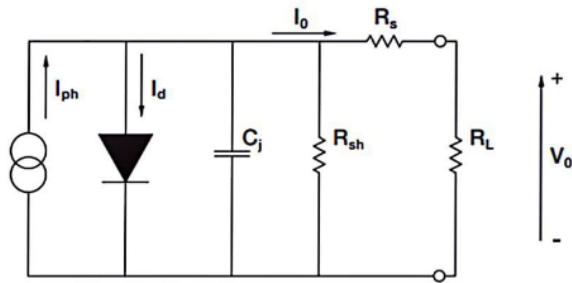


Fig. 4 Equivalent PD Circuit Model

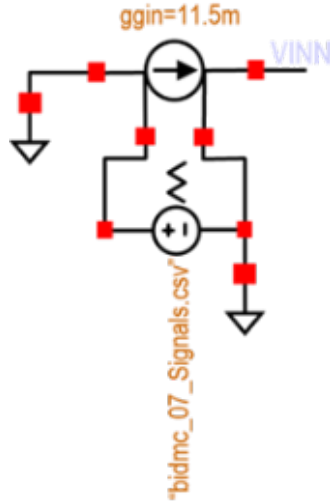


Fig. 5 PWL Source which generates PPG signal

2.3 Self-biased Two-stage Miller OTA

The core operational amplifier (op-amp) of the Transimpedance Amplifier TIA is Self-biased Two-stage Miller OTA. In this work, the Miller amplifier achieved an open loop gain of 89dB and Bandwidth equal to 74KHz, see Fig. 6.

The phase margin is 77° and the offset voltage is $1.8 \mu\text{V}$. The load capacitor used is 4pF with bias current equal to 80nA. The slew rate is $0.038\text{V}/\mu\text{s}$ and the output voltage is 811mV. The Common Mode Rejection Ratio (CMRR) is 96.6dB and the Power Supply Rejection Ratio (PSRR) is 111dB, as shown in Table 1.

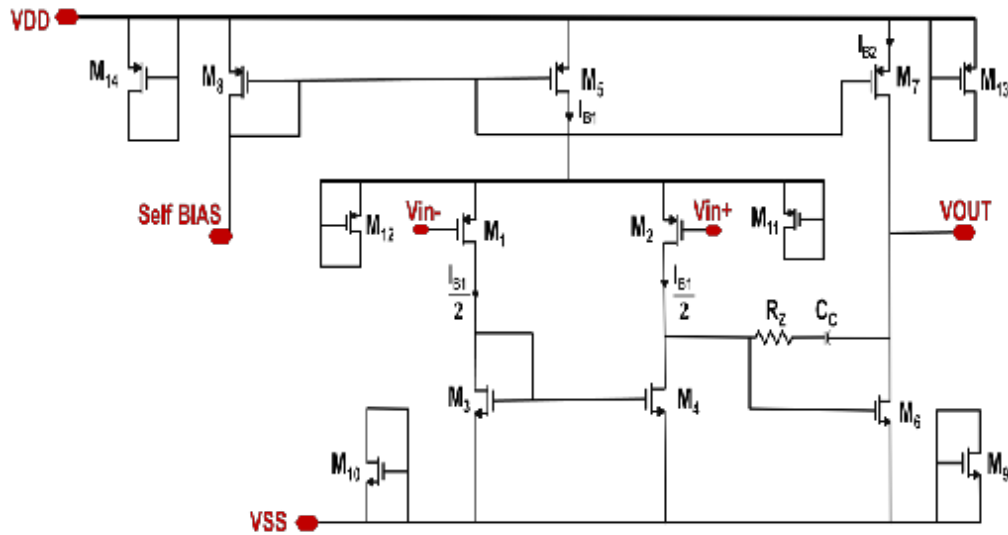


Fig. 6 Miller Amplifier Schematic

Table1 Two stage miller PMOS input pair sizing

| | g_m/I_D | L | W |
|----------|-----------|-----------|-----------|
| M1, M2 | 21.5 | 1 μ | 500n |
| M3, M4 | 23.9 | 2.1 μ | 1.1 μ |
| M5 | 19.03 | 1 μ | 500n |
| M6 | 23.9 | 2.1 μ | 1.1 μ |
| M7 | 19.6 | 1 μ | 500n |
| M8 | 19.7 | 1 μ | 500n |
| M9, M10 | 0 | 2.1 μ | 1.1 μ |
| M11, M12 | 0 | 1 μ | 500n |
| M13, M14 | 0 | 1 μ | 500n |

2.4 Constant gm Biasing Circuit

The Biasing current is implemented as a function of temperature, see Fig. 7 and Table 2, from -25°C to 40°C and the temperature coefficient is calculated as:

$$TC = \frac{I_{max} - I_{min}}{(I_{nom}(T_{max} - T_{min}))} * 10^6 \quad (3)$$

T_{max} and T_{min} equal -25°C and 40°C respectively. I_{nom} is the current at nominal temperature. The Tc of output current is $1779.5\text{ppm}/^\circ\text{C}$.

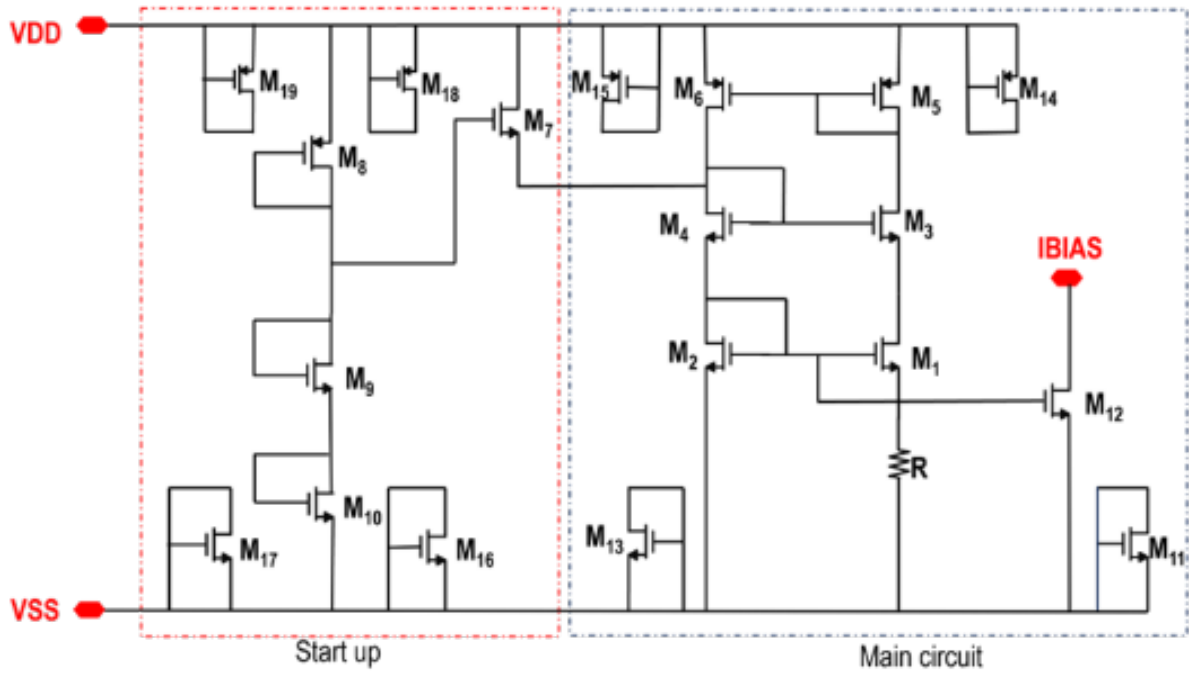


Fig. 7 Constant gm circuit Schematic and start up circuit

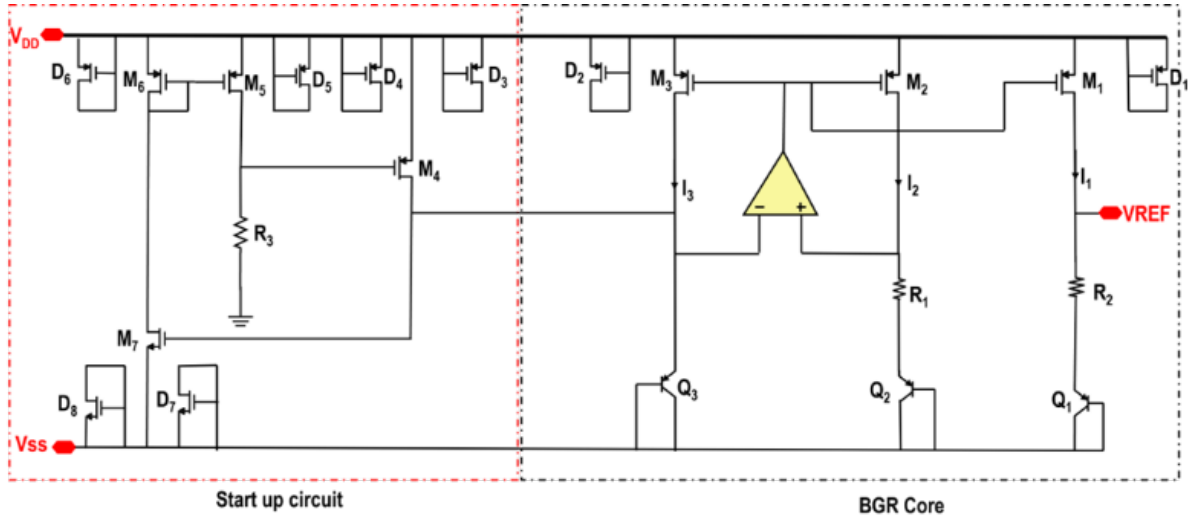
Table 2 Sizing of gm constant with start-up circuit

| | L | W |
|----------|----------|----------|
| M1 | 1 μ | 500n |
| M2 | 1 μ | 500n |
| M3, M4 | 1 μ | 500n |
| M5, M6 | 1 μ | 500n |
| M7, M8 | 1 μ | 220n |
| M9, M10 | 1 μ | 220n |
| M11, M13 | 1 μ | 500n |
| M12 | 1 μ | 500n |
| M14, M15 | 1 μ | 500n |

2.5 Bandgap Reference Circuit

Bandgap reference (BGR) is used to generate a stable temperature-independent reference voltage. In this work, the reference voltage (VREF) is equal to 1.249V. The change in voltage levels (ΔV_{ref}) with temperature variation is 0.2m while the temperature sweep range is from -40 °C to 125 °C and the Temperature Coefficient (TC) is 4.36 ppm/c. The Power Supply Rejection Ratio (PSRR) is about 47dB.

The line regulation is calculated, it is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage, see Fig. 8.

**Fig. 8** Bandgap Reference circuit

$$\text{Line Regulation} = \frac{\Delta V_{REF}}{\Delta V_{DD}} = \frac{1.25}{1.8} = 0.69 \quad (4)$$

$$\text{Load Regulation} = \frac{\Delta V_{REF}}{\Delta I_O} = \frac{1.25}{10\mu} = 0.125\text{v/uA} \quad (5)$$

To operate the circuit under normal conditions and prevent the wrong equilibrium point, a startup circuit is necessary. The bandgap reference circuit functions normally when the voltages at the two input nodes of the op-amp

are equal. Therefore, during a zero current state (when I_o is zero), the voltages at both the inverting and non-inverting terminals of the op-amp are 0V, which is a stable state for the op-amp and allows the BGR circuit to lock into place. During zero current state voltage at the inverting terminal of op-amp is 0V thus transistor N1 turns off causing zero current to flow through transistor P1 which is mirrored to transistor P2 causing transistor P3 to turn on providing current to resistance R of 350K to generate a higher voltage which triggers the 0V state of an op-amp and op-amp goes in normal operation, shown in Table 3.

Table 3 BGR Sizing of resistors, Mosfets and BJTs.

| | L | W |
|------------|---------------------------------|---------------------------------|
| M1, M2, M3 | 2 μ | 10 μ |
| Mp1, Mp2 | 800 n | 600 n |
| Mp3 | 500 n | 600 n |
| MN1 | 1 μ | 1 μ |
| D1, D2 | 2 μ | 10 μ |
| D3, D4 | 500 n | 600 n |
| D5, D6 | 800 n | 600 n |
| D7, D8 | 1 μ | 1 μ |
| | Sum L(μm) | Sum W(μm) |
| | 9.595 | 2 |
| | 99.3 | 2 |
| | Multiplier | Emitter area |
| Q1, Q3 | 1 | $1 \times 10^{(-10)}$ |
| Q2 | 8 | $1 \times 10^{(-10)}$ |

2.6 Voltage to current transducer Circuit

A voltage-to-current converter, known as a voltage-to-current transducer, is used to provide a wide range of output current levels, from milliamps to amps. In this work, the input voltage range is from 0 to 1.8V while the output voltage level is half of it, 0.9V or 900mV, as shown in Table 4. For PVT results of the voltage-to-current converter, the Nominal output voltage is 900mV, Minimum output voltage 897.7mV and Maximum output voltage is 900.3mV, see Fig. 9.

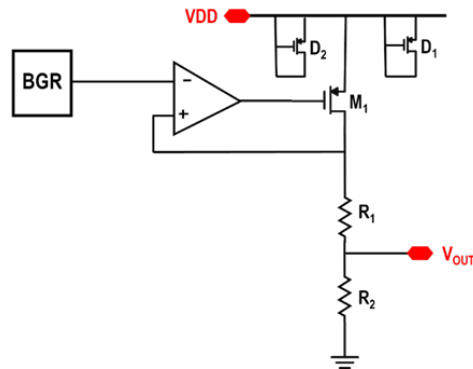


Fig. 9 V-to-I Circuit

In our design we assume that $R_2 = 1M$ and from voltage divider we calculate R_1 as shown in (Eq 4)

$$V_{out} = 1.25 \times \frac{R_2}{R_1 + R_2} \quad (6)$$

Table 4 Voltage to current converter sizing.

| | L | W |
|--------|--------------|------------------|
| M1 | 1 u | 450 n |
| D1, D2 | 1 u | 450 n |
| | Sum L | Sum W(μm) |
| R1 | 695.435 u | 2 |
| R2 | 1.79102 m | 2 |

2.7 IDAC for DC Current Cancellation

The signal baseline is affected by motion artifacts, micro motions between the skin and artery, ambient light, and tissue absorption of light. IDAC is a digitally controlled current source, a digital controller with switches connected to current mirror MOSFETs to produce the current which steers the DC current from the Photodiode to prevent saturation or signal distortion, see Fig. 10.

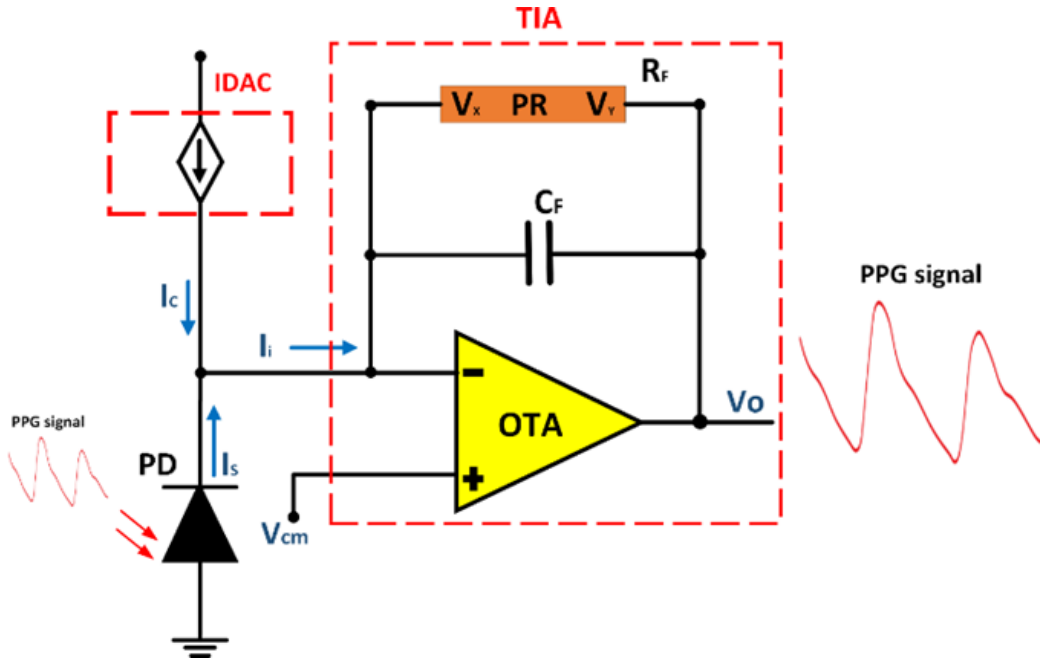


Fig. 10 AFE Circuit with IDAC Cancellation

Testing IDAC itself with load ($R = R_f$ and $C = C_f$ of TIA) without the existence of the PPG signal, by applying the 4 output cases from the controller, see Fig. 11.

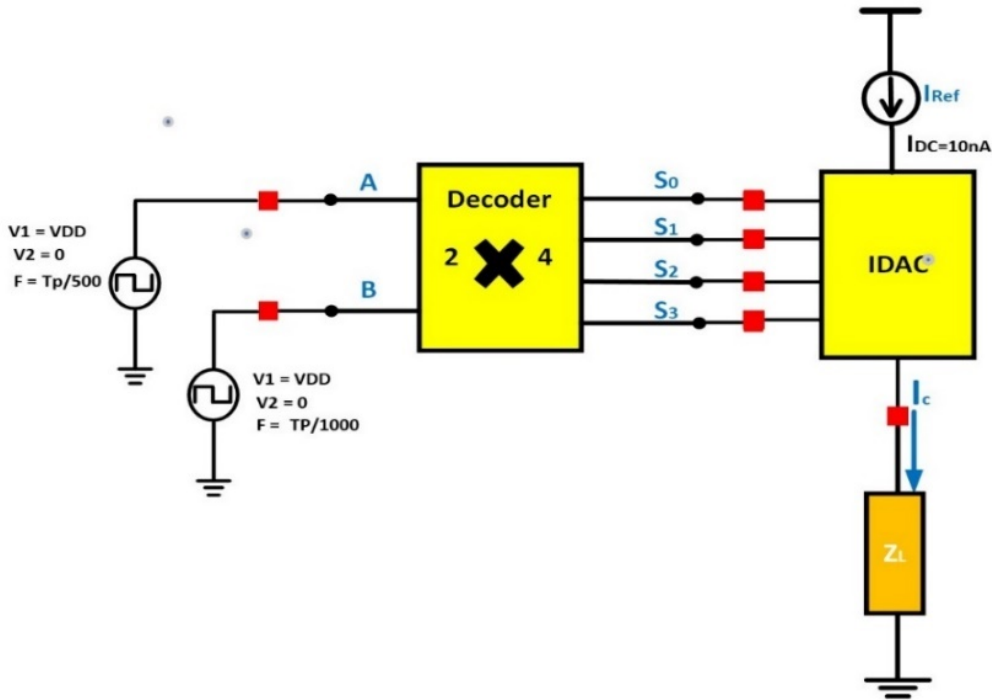


Fig. 11 Testing IDAC

IDAC produces DC equal to the DC of the PPG signal, a sum of current sources controlled by the digital controller, see Fig. 12.

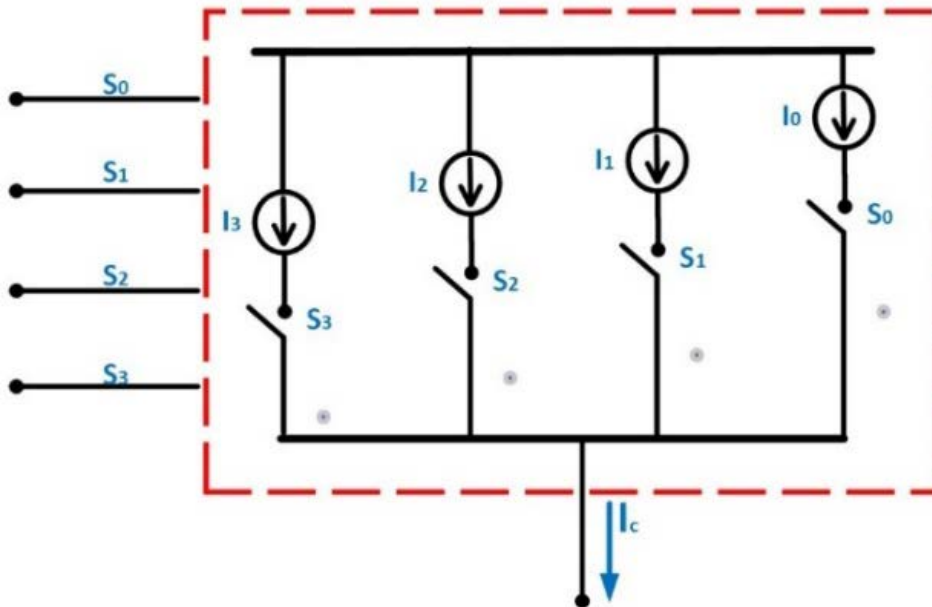


Fig. 12 Switching Controlled Current sources

For the decoder Implementation, Pins S0, S1, S2 and S3 represent the voltage applied on switches to control its state. D0 is the least significant bit (LSB) in our case as 00 input activate it, see Fig. 13.

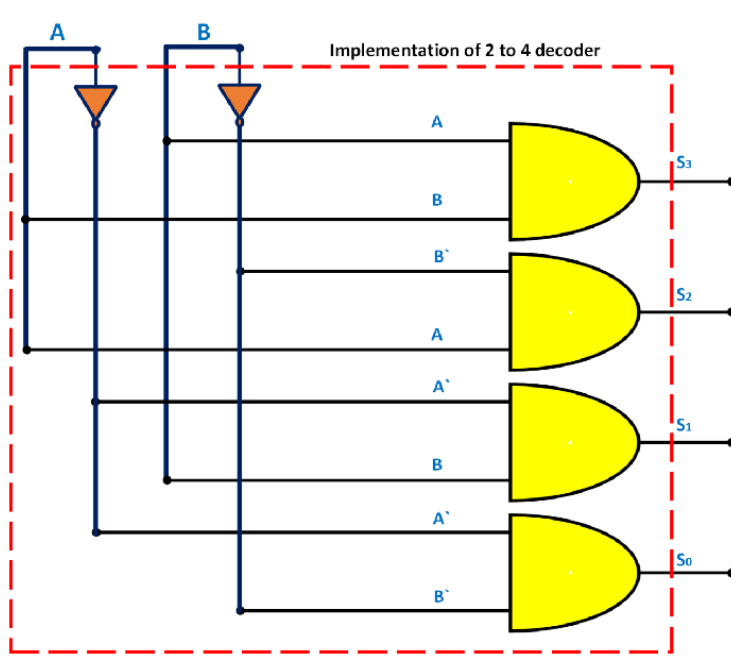


Fig. 13 Decoder Schematic

For design of AND gate, as we rely on current mirroring, all lengths must be equal to achieve better matching. let $L=1\mu\text{m}$. The widths will increase exponentially by a factor of 2. The reference current will be 10nA , and the current sensing range will be up to 80nA , see Fig. 14.

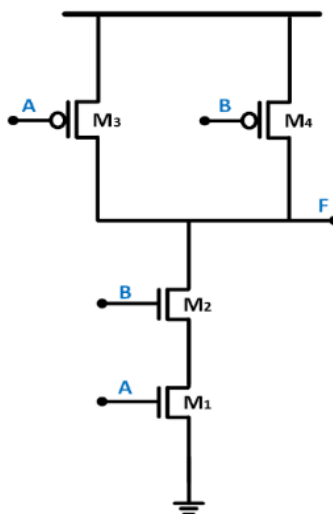


Fig. 14 AND Gate

NMOS M1 and PMOS M3 are crucial in design. To handle nano currents, a large gm/Id is necessary to achieve the desired current density while maintaining a minimum MOS width of 500nm to reduce PVT (Process, Voltage, and Temperature) variations. The sizing ratio W/L can be factored in to achieve accurate mirroring ratios, as shown in Table 5 and Fig. 15.

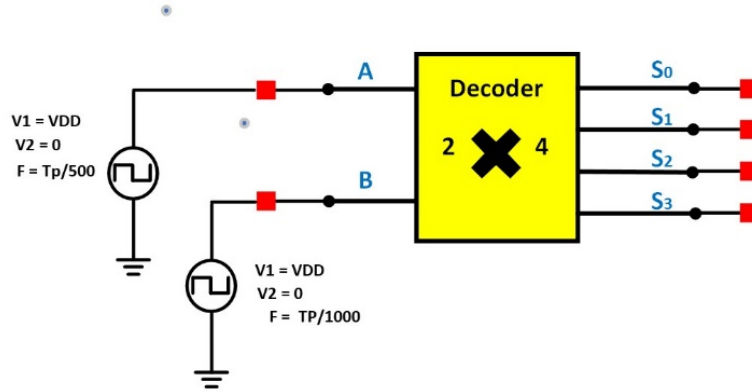


Fig. 15 Testing the decoder functionality

This truth table illustrates possible input cases and their relationship with outputs.

Table 5 Truth table of controller function.

| Inputs | | Outputs | | | |
|--------|---|---------|----|----|----|
| A | B | S0 | S1 | S2 | S3 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Current produced from IDAC depends on the control signal from the controller, see Fig. 16.

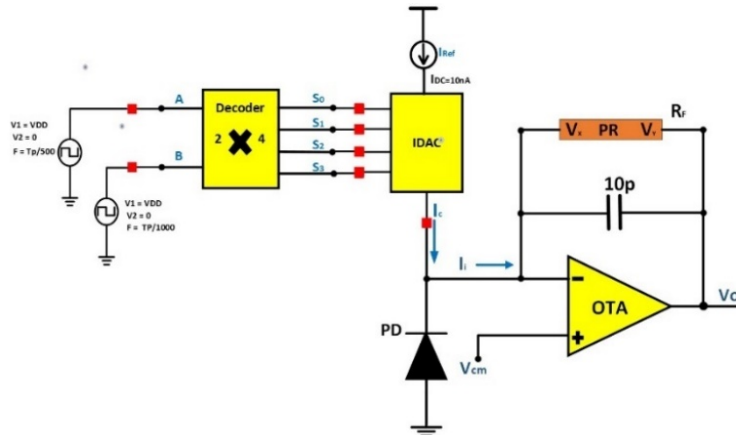


Fig. 16 Complete Cancellation System

3. Physical Layout Design

Self-biased Two stage Miller Op-Amp, Bandgap Reference (BGR), voltage-to-current converter (V-I) and Transimpedance Amplifier (TIA) layout are done using virtuoso layout editor tool and caliber tools from Mentor Graphics, see Figs. 17-20. Design Rule Check (DRC), Layout Versus Schematic (LVS), Parasitic Extraction (PEX), and post-layout simulation are all provided by these tools. To minimize parasitic factors that could alter the circuit's behaviors, this arrangement was carefully executed. Electrostatic discharge (ESD), latch-up, layout dependent proximity effects (LDPEs), matching techniques (MTs), and electro-migration (EM) are just a few of the difficulties that are studied. Completely layout area of the Self-biased Two stage Miller Op-Amp PMOS input pair [99.355 x 76.44] (μm^2), Bandgap Reference (BGR) [178 x 99.68] (μm^2), voltage-to-current converter (V-I) [319.2 x 99.63] (μm^2), Transimpedance Amplifier (TIA) [445.14 x 99.63] (μm^2).

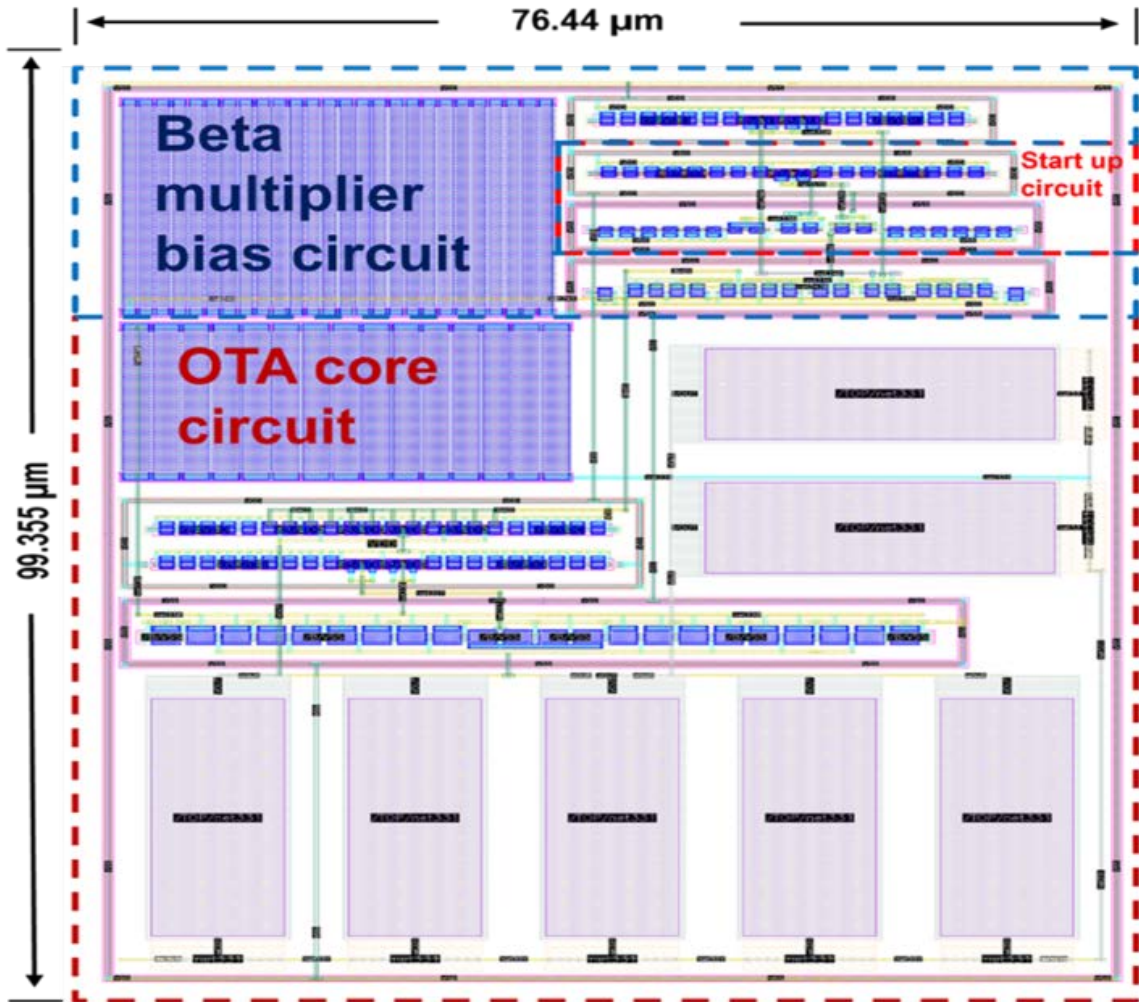


Fig. 17 Self-biased op-Amp Layout.

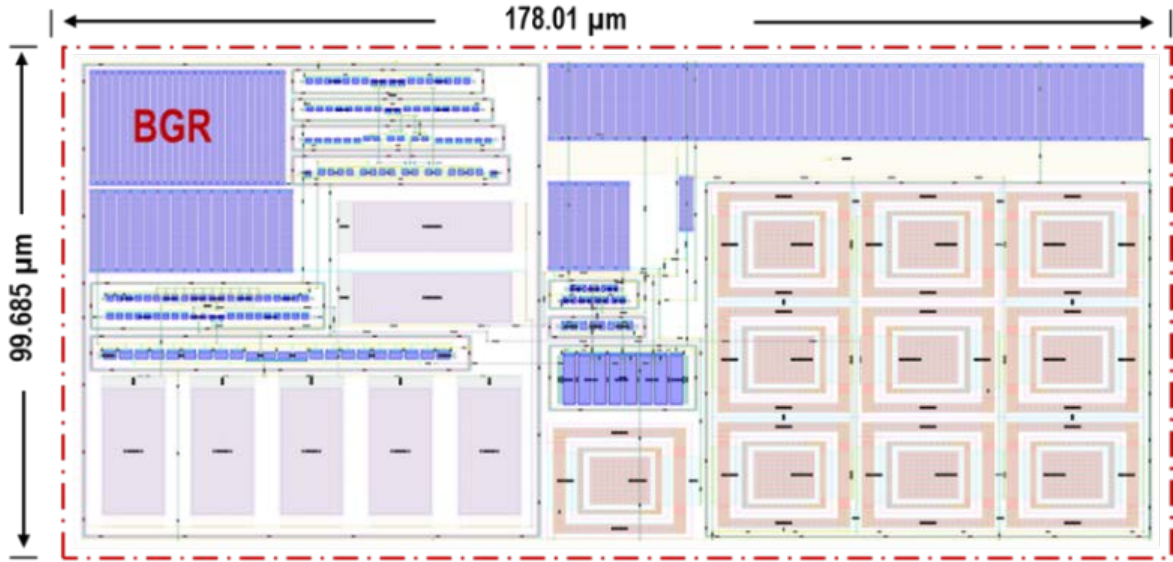


Fig. 18 Bandgap Reference Layout.

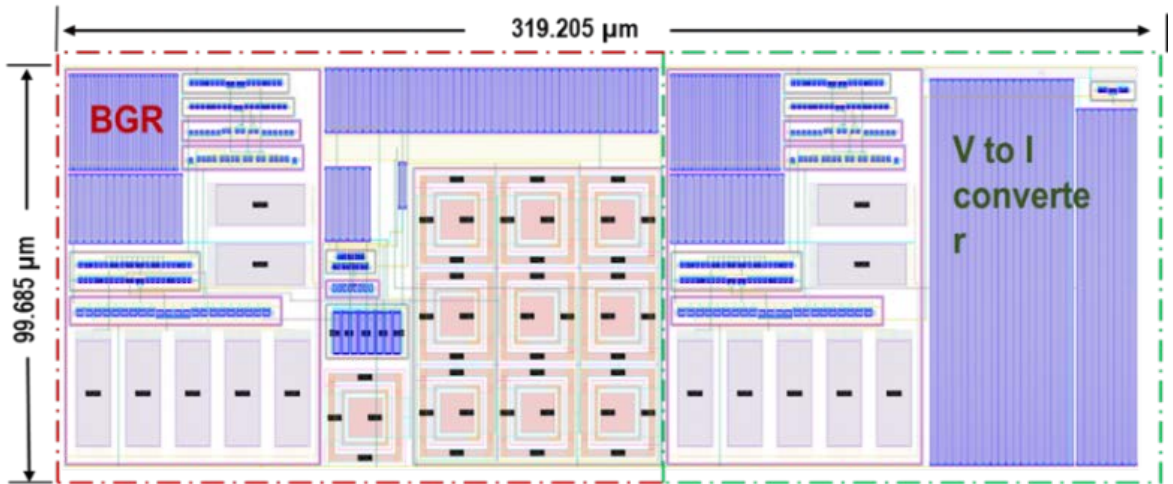


Fig. 19 Voltage-to-current Layout.

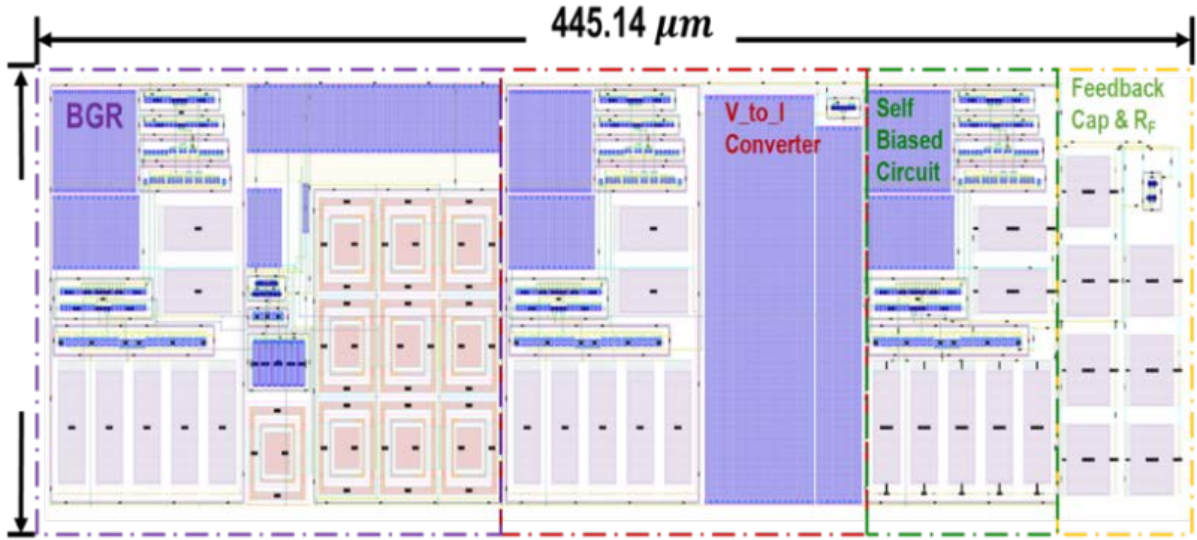


Fig. 20 Transimpedance Amplifier Layout.

4. Simulation Results

4.1 Self-biased Miller OTA

In Fig 21, AC analysis for the self-biased two-stage Miller involves sweeping frequencies from 1 Hz to 10 GHz with an input differential voltage of 1V AC magnitude. The frequency response indicates a DC open-loop gain of 89.048 dB, a bandwidth of 2 Hz, and a gain-bandwidth product of 74 kHz, see Fig. 21.

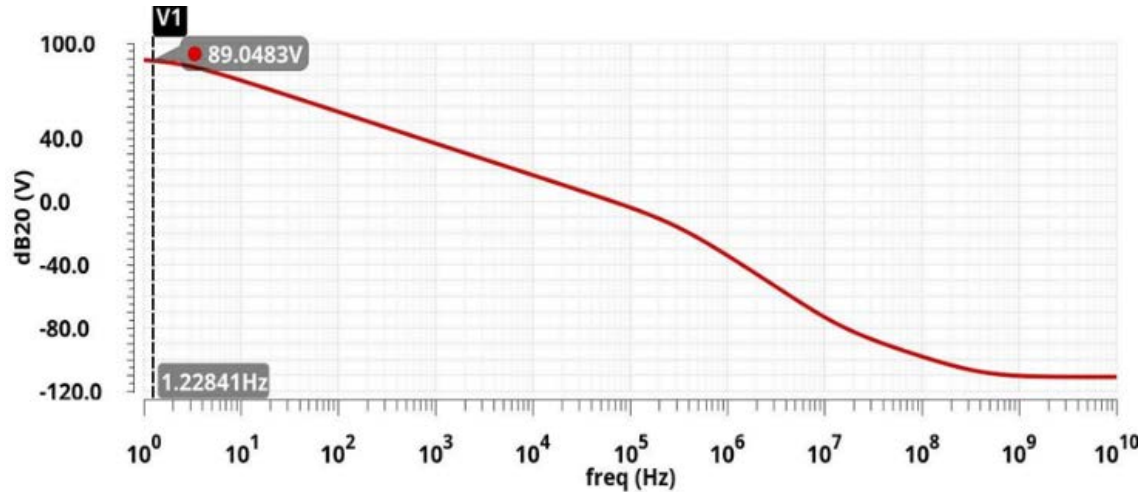


Fig. 21 Frequency response of Miller OTA.

PSRR+ is 111.058 dB. The curve is generated using AC analysis, where the differential output voltage is divided by the supply voltage, see Fig. 22.

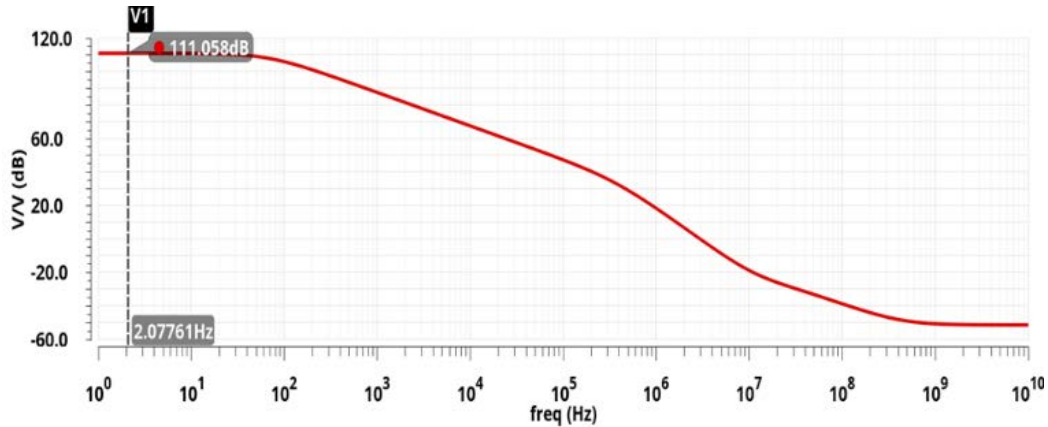


Fig. 22 Open loop simulation result PSRR+

Loop gain is plotted using STP analysis. The OTA in a unity feedback network, the loop gain equals the open-loop gain, which is 89 dB, with a phase margin of 77°, see Fig. 23.

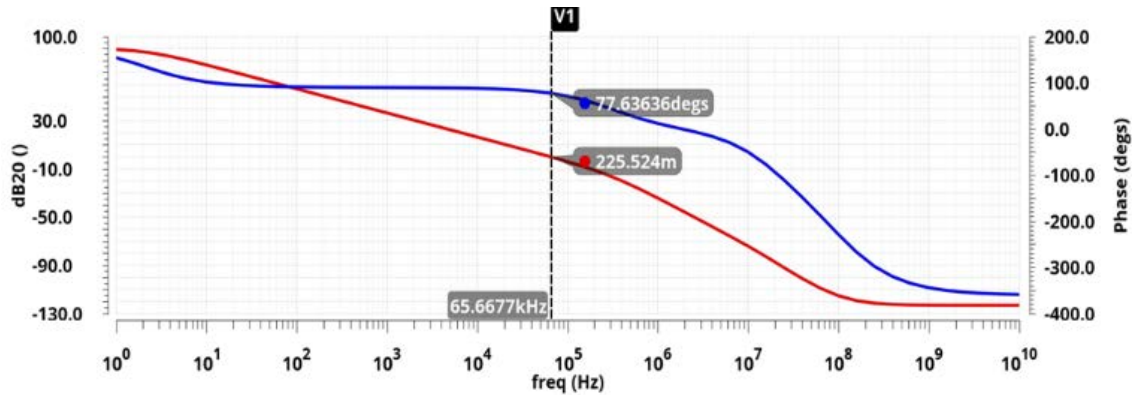


Fig. 23 Loop gain Vs frequency and phase Vs frequency

The slew rate is plotted by using transient analysis and use step voltage in input voltage and setting $v_1=250\text{mV}$, $v_2=950\text{mV}$, period=1s and pulse width =1s. The slew rate is $0.038\text{ V}/\mu\text{s}$, see Fig. 24 and Fig. 25.

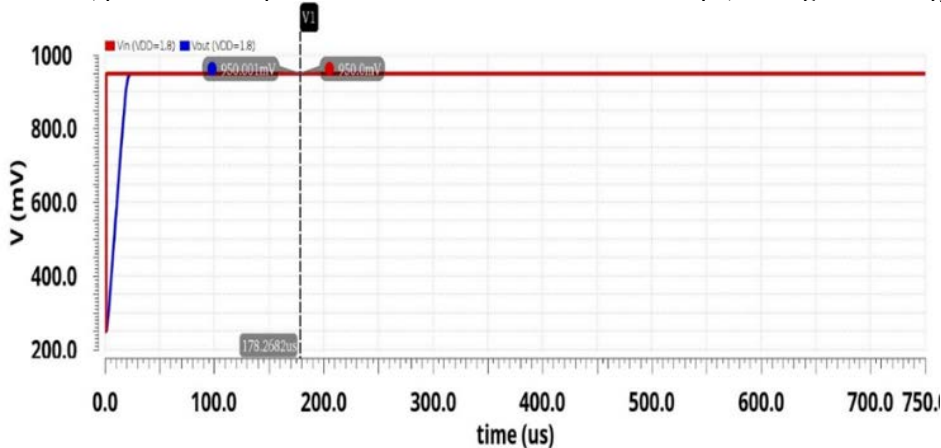


Fig.24 step response simulation results

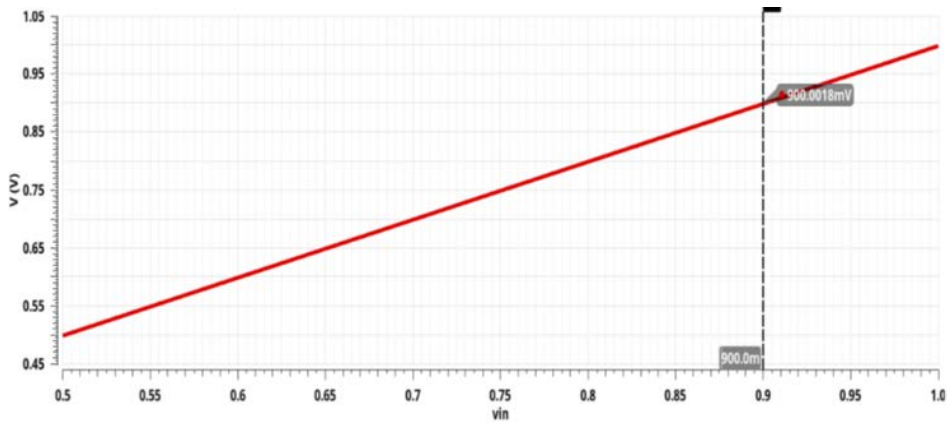


Fig.25 Offset of Miller OTA

4.2 Biasing Circuit

The Biasing Current is implemented as a function of supply voltage and shown that Biasing current is saturated at the voltage from 0.9 to 1.8V, see Fig. 26 and Fig. 27.

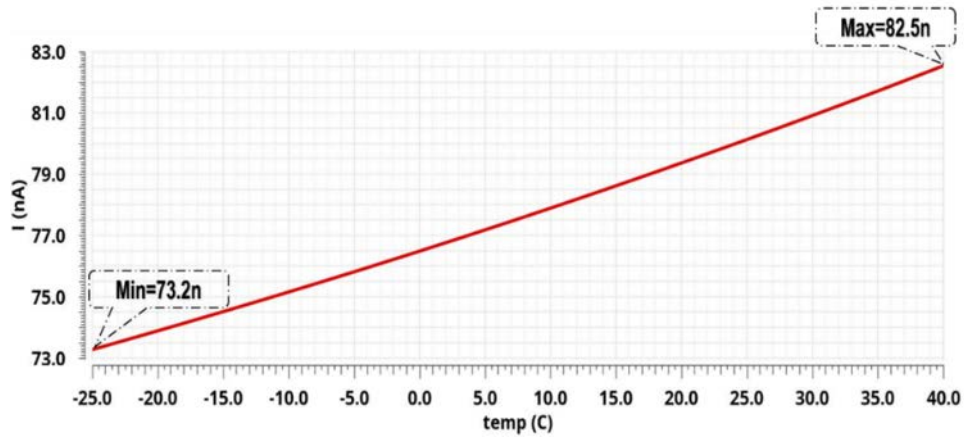


Fig.26 Current with Temperature.

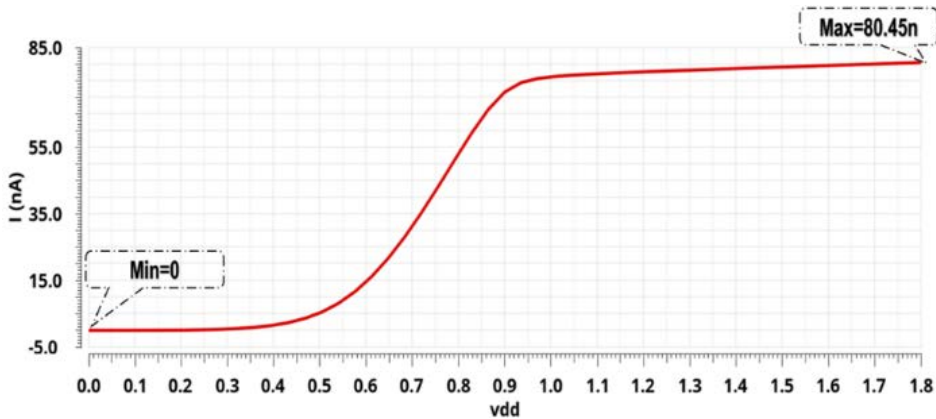


Fig.27 Current vs Power supply

4.3 Bandgap Reference Circuit

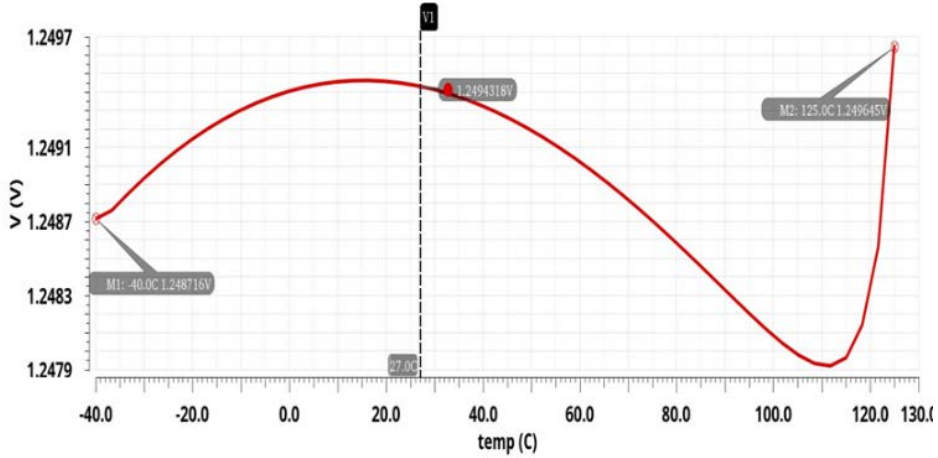


Fig. 28 V_{REF} vs. temperature

In Fig.28 the positive temperature coefficient is PTAT that increases with temperature, negative temperature coefficient is CTAT voltage that decreases with temperature and reference voltage is constant with temperature, See Figs. 29-31.

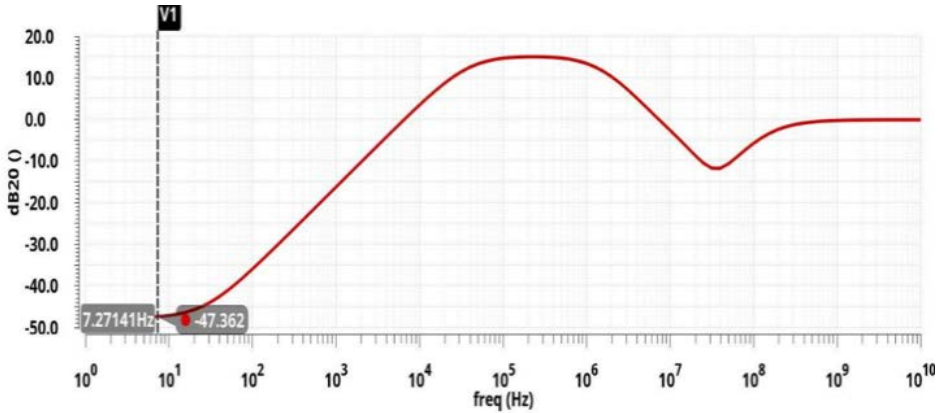


Fig. 29 PSRR of the bandgap reference circuit

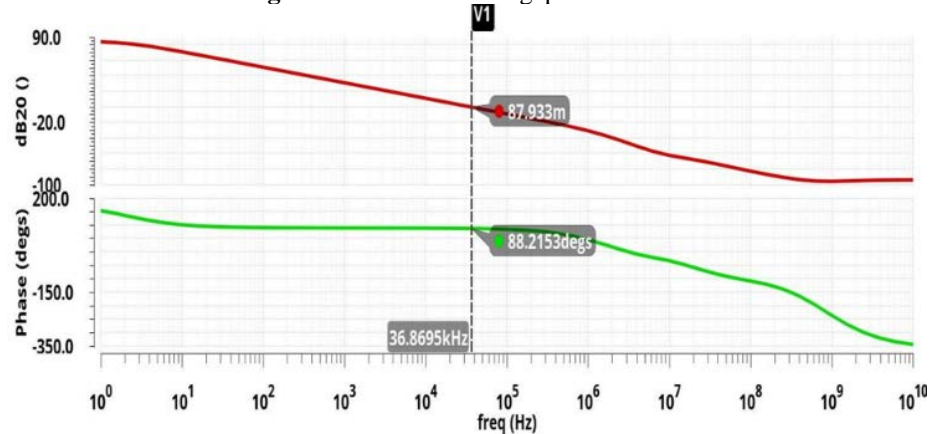
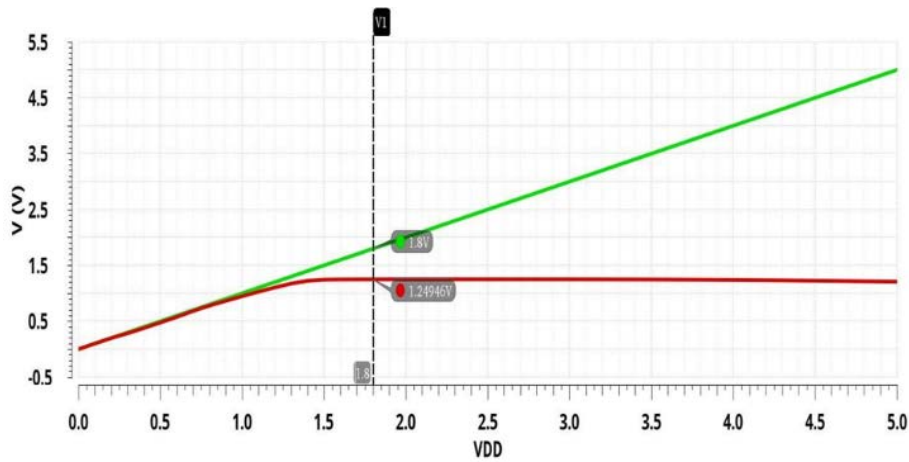
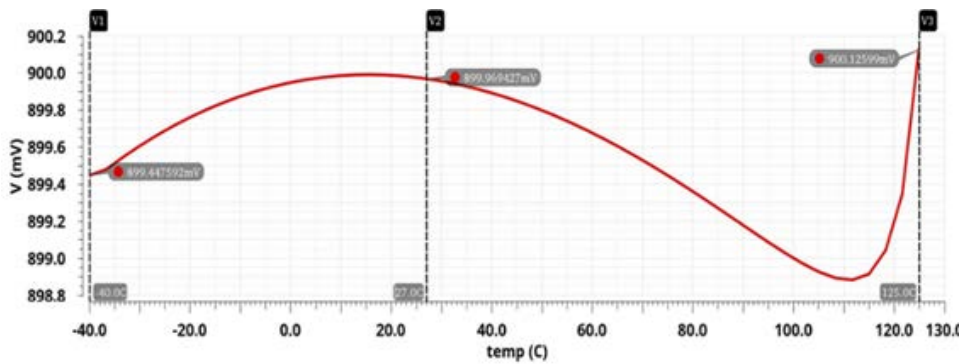
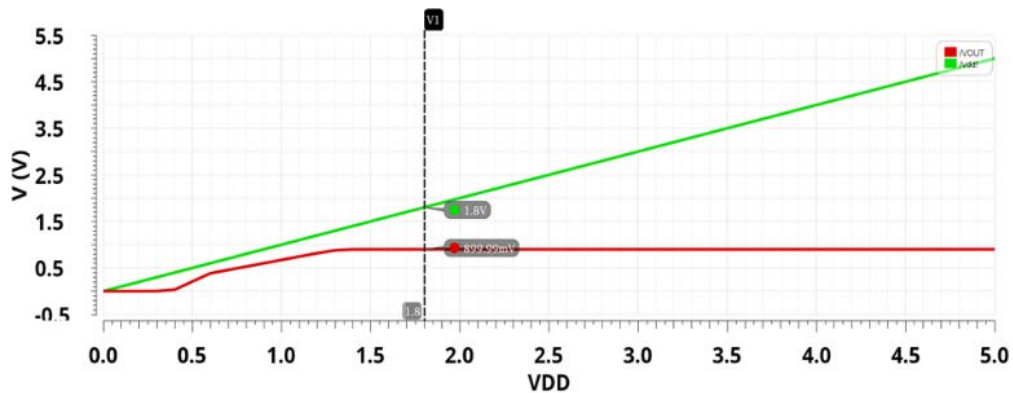


Fig. 30 Loop gain and phase of Bandgap Reference.

Fig. 31 V_{REF} vs. V_{DD}

4.4 Voltage-to-current Converter

In Fig. 32 the reference voltage is plotted while sweeping the supply voltage over a wide range from 0 v to 5 v. This indicates that the reference voltage remains constant over this range of supply voltages and saturates at 899.99 mV, see Figs. 33-34.

Fig. 32 V_{out} vs. temperature.Fig.33 V_{out} vs. V_{DD} .

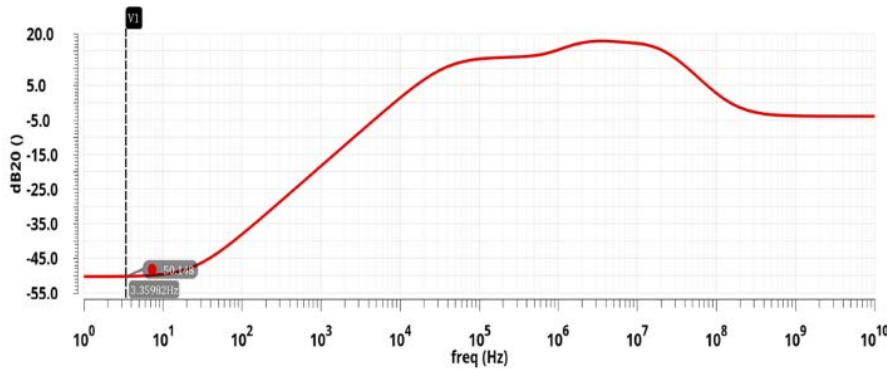


Fig.34 PSRR of voltage to current converter circuit

Table 6 Comparison with recently published work

| | [26] | [41] | [42] | [43] | This work |
|-------------------|-------|---------|---------|---------|-----------|
| Technology nm | 90 | 180 | 65 | 65 | 180 |
| Supply voltage | - | - | 1.2 | 2.4 | 1.8 |
| C_{pd} | 0.3pF | 0.5pF | 1400 fF | 70 fF | 10 pF |
| Gain/dBΩ | 63.5 | 60.5 | 51-73 | 51 | 143.542 |
| Bandwidth | 6 GHz | 5.2 GHz | 0.55GHz | 8-12GHz | 6.874kHz |
| Power dissipation | 12mW | 28mW | 4.8mW | 0.26mW | 1.49nW |

This paper focused on the design of the analog front end (AFE) for a PPG sensor in wearable technology, future work can encompass several advanced areas to enhance the performance and applicability of the sensor. One key direction is the optimization for power efficiency, which involves reducing the power consumption of the AFE to extend battery life in wearable devices. This can be achieved through low-power design techniques and exploring energy harvesting methods, such as using body heat or motion to power the sensor, shown in Table 6.

Another important area is enhanced signal processing. Developing advanced noise reduction algorithms and implementing adaptive filtering techniques can significantly improve the quality of the PPG signal, especially in dynamic environments with varying noise conditions [44]. Additionally, integrating the PPG sensor with other physiological sensors, such as ECG or accelerometers, can provide more comprehensive health monitoring and improve measurement accuracy. Miniaturization and integration are also crucial for future work. This includes developing a System-on-Chip (SoC) that integrates the AFE with other components to reduce size and improve reliability.

5. Conclusion

This paper involves designing a low-power PPG sensor circuit for cardiovascular monitoring. The Analog Front-End (AFE) in 0.18 μm CMOS amplifies weak photocurrents using a Transimpedance Amplifier (TIA) and operates in the subthreshold region to minimize power consumption. A DC current cancellation loop to manage large DC photocurrent.

The TIA, with a self-biased two-stage Miller OTA and Bandgap Reference (BGR), converts weak photocurrents to amplified voltages, ensuring stable output despite supply fluctuations. Pseudo-resistance provides high gain with a small chip area, and an IDAC controlling circuit cancels DC offset, enhancing dynamic range.

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References

- [1] J. L. Moraes et al., "Advances in photoplethysmography signal analysis for biomedical applications," *Sensors*, vol. 18, no. 6, p. 1894, Jun. 2018. doi:10.3390/s18061894
- [2] Z. Ebrahimi and B. Gosselin, "Ultralow-power photoplethysmography (PPG) sensors: A methodological review," *IEEE Sensors Journal*, vol. 23, no. 15, pp. 16467–16480, Aug. 2023. doi:10.1109/jsen.2023.3284818
- [3] R. Finnerty, "How to design a better pulse oximeter," *Analog Devices*, <https://www.analog.com/en/resources/technical-articles/how-to-design-a-better-pulse-oximeter.html> (accessed Jun. 19, 2024).
- [4] A. Atef, M. Atef, E. E. Khaled, and M. Abbas, "CMOS transimpedance amplifiers for biomedical applications: A comparative study," *IEEE Circuits and Systems Magazine*, vol. 20, no. 1, pp. 12–31, 2020. doi:10.1109/mcas.2019.2961724
- [5] Dey, N., Ashour, A.S., Mohamed, W.S., Nguyen, N.G. (2019). *Biomedical Signals*. In: *Acoustic Sensors for Biomedical Applications*. SpringerBriefs in Speech Technology. Springer, Cham. https://doi.org/10.1007/978-3-319-92225-6_2
- [6] K. Ing, "Design and experimentation of wearable body sensors," *Rapid Prototyping Technology - Principles and Functional Requirements*, Sep. 2011. doi:10.5772/19857
- [7] S. Ryals et al., "Photoplethysmography—new applications for an old technology: A sleep technology review," *Journal of Clinical Sleep Medicine*, vol. 19, no. 1, pp. 189–195, Jan. 2023. doi:10.5664/jcsm.10300
- [8] Q. Lin, J. Xu, S. Song, A. Breeschoten, M. Konijnenburg, C. Van Hoof, F. Tavernier, and N. Van Helleputte, "A 119db dynamic range chargecounting light-to-digital converter for wearable ppg/nirs monitoring applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 14, no. 4, pp. 800–810, 2020.
- [9] K. Sasai et al., "A low-power photoplethysmography sensor using correlated double sampling and reference readout circuit," *2019 IEEE SENSORS*, Oct. 2019. doi:10.1109/sensors43011.2019.8956852
- [10] B. Lin, M. Atef, and G. Wang, "14.85 μ W analog front-end for photoplethysmography acquisition with 142-dB gain and 64.2-pA rms noise," *Sensors*, vol. 19, no. 3, p. 512, Jan. 2019. doi:10.3390/s19030512
- [11] Z. Zhou and P. Warr, "Feedback controlled pseudo resistor," *Electronics Letters*, vol. 56, no. 8, pp. 371–373, Apr. 2020. doi:10.1049/el.2019.3779
- [12] R. K. Pandey, T.-Y. Lin, and P. C.-P. Chao, "Design and implementation of a photoplethysmography acquisition system with an optimized artificial neural network for accurate blood pressure measurement," *Microsystem Technologies*, vol. 27, no. 6, pp. 2345–2367, Jan. 2021. doi:10.1007/s00542-020-05109-9
- [13] R. Y., "What is a photodiode? definition, principle, construction, working, characteristics, advantages, disadvantages and applications of Photodiode," *Circuit Globe*, <https://circuitglobe.com/photodiode.html> (accessed Jun. 25, 2024).
- [14] F. Saffih, "Artificially-Intelligent Imaging (AI2) sensors: How intelligent CMOS imaging devices can benefit photovoltaics?" *2017 7th International Conference on Modeling, Simulation, and Applied Optimization (ICMSAO)*, Apr. 2017. doi:10.1109/icmsao.2017.7934899
- [15] Atef, M., Zimmermann, H. (2016). *Optoelectronic Circuits in Nanometer CMOS Technology*. In: *Optoelectronic Circuits in Nanometer CMOS Technology*. Springer Series in Advanced Microelectronics, vol 55. Springer, Cham. https://doi.org/10.1007/978-3-319-27338-9_10
- [16] L. Orozco, *Programmable-Gain Transimpedance Amplifiers Maximize Dynamic Range in Spectroscopy Systems* | *Analog Devices*, <https://www.analog.com/en/resources/analog-dialogue/articles/programmable-gain-transimpedance-amplifiers.html> (accessed Jun. 26, 2024).
- [17] A. K. Sharma et al., "Common-Centroid Layouts for Analog Circuits: Advantages and Limitations," *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, 2021, pp. 1224–1229, doi: 10.23919/DATE51398.2021.9474244.
- [18] T. Hashimoto, H. Satoh, H. Fujiwara and M. Arai, "A Study on Suppressing Crosstalk Through a Thick SOI Substrate and Deep Trench Isolation," in *IEEE Journal of the Electron Devices Society*, vol. 1, no. 7, pp. 155–161, July 2013, doi: 10.1109/JEDS.2013.2279677.
- [19] Li-Da Huang and M. D. F. Wong, "Optical proximity correction (OPC)-friendly maze routing," *Proceedings. 41st Design Automation Conference*, 2004., San Diego, CA, USA, 2004, pp. 186–191.
- [20] J. Mahattanakul and J. Chutichatuporn, "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 8, pp. 1508–1514, Aug. 2005, doi: 10.1109/TCSI.2005.851395.
- [21] X. Ming, Y. -q. Ma, Z. -k. Zhou and B. Zhang, "A High-Precision Compensated CMOS Bandgap Voltage Reference Without Resistors," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 10, pp. 767–771, Oct. 2010, doi: 10.1109/TCSII.2010.2067770.
- [22] A. Becker-Gomez, T. Lakshmi Viswanathan and T. R. Viswanathan, "A Low-Supply-Voltage CMOS Sub-Bandgap Reference," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 7, pp. 609–613, July 2008, doi: 10.1109/TCSII.2008.921580.
- [23] B. Fotouhi, "All-MOS voltage-to-current converter," in *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 147–151, Jan. 2001, doi: 10.1109/4.896241.

- [24] M. Mansuri and C. -K. K. Yang, "A low-power adaptive bandwidth PLL and clock buffer with supply-noise compensation," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 11, pp. 1804-1812, Nov. 2003, doi: 10.1109/JSSC.2003.818300.
- [25] Lin, Q., Sijbers, W., Avidikou, C., Van Hoof, C., Tavernier, F., & Van Helleputte, N. (2022). Photoplethysmography (PPG) Sensor Circuit Design Techniques. 2022 IEEE Custom Integrated Circuits Conference (CICC).
- [26] M. Atef et al: "8Gbits/s inductorless transimpedance amplifier in 90 nm CMOS technology," *Analog Integrated Circuits and Signal Processing* 79 (2014) 27
- [27] Kim, J., Kim, J., & Ko, H. (2015). Low-power photoplethysmogram acquisition integrated circuit with robust light interference compensation. *Sensors*, 16(1), 46.
- [28] Güngördü, A. D., DüNDAR, G., & Yelten, M. B. (2020b). A high performance TIA design in 40 NM CMOS. 2020 IEEE International Symposium on Circuits and Systems (ISCAS).
- [29] Razavi, B. (2023). The design of a Transimpedance amplifier [the analog mind]. *IEEE Solid-State Circuits Magazine*, 15(1), 7–11.
- [30] Salem, A. M., Wahba, A., Hamed, H. F. A., & Mohamed, A. R. (2024). A pseudo resistor with temperature self-adaptive scheme. *Integration*, 98, 102229.
- [31] Sharma, K., Pathania, A., Pandey, R., Madan, J., & Sharma, R. (2021). MOS based pseudo-resistors exhibiting Tera Ohms of incremental resistance for biomedical applications: Analysis and proof of concept. *Integration*, 76, 25–39.
- [32] Djekic, D., Fantner, G., Behrends, J., Lips, K., Ortmanns, M., & Anders, J. (2017). A transimpedance amplifier using a widely tunable PVT-independent pseudo-resistor for high-performance current sensing applications. *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*.
- [33] Lin, B., Atef, M., & Wang, G. (2019). 14.85 μ W analog front-end for photoplethysmography acquisition with 142-dB ω gain and 64.2-pArms noise. *Sensors*, 19(3), 512.
- [34] AbuShawish, I. Y., Mahmoud, S. A., Majzoub, S., & Hussain, A. J. (2023b). Biomedical amplifiers design based on pseudo-resistors: A Review. *IEEE Sensors Journal*, 23(14), 15225–15238.
- [35] AbuShawish, I. Y., Mahmoud, S. A., Majzoub, S., & Hussain, A. J. (2023b). Biomedical amplifiers design based on pseudo-resistors: A Review. *IEEE Sensors Journal*, 23(14), 15225–15238.
- [36] Roger Yubtzuan Chen, I Seng-Fong Lin, I and Ming-Shian Wu I, A Linear CMOS voltage – to current converter Circuits Systems Signal Processing vol. 25, no. 4, 2006, PP. 497–509.
- [37] M. Mansuri and C.-K. K. Yang, A low-power adaptive bandwidth PLL and clock buffer with supply-noise compensation, *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1804–1812, November 2003.
- [38] Ming, Xin, Ying-qian Ma, Ze-kun Zhou, and Bo Zhang, "A high-precision compensated CMOS bandgap voltage reference without resistors" ,*IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 10, pp. 767-771, Oct 2010.
- [39] MingZhe Zhang "Design of A Low Power Dissipation Bandgap Voltage Reference Without Resistors." *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)* 13.1 (2018): 66-72.
- [40] Mahattanakul, J., & Chutichatuporn, J. (2005). Design procedure for two-stage CMOS OPAMP with flexible noise-power balancing scheme. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(8), 1508–1514.
- [41] Xie, S., Wu, S., Mao, L., & Li, H. (2017). A design methodology to extend bandwidth for regulated Cascode Transimpedance amplifier. *IEICE Electronics Express*, 14(2), 20161098–20161098.
- [42] Jeong, G.-S.; Chi, H.; Kim, K.; Jeong, D.-K. A 20-Gb/s 1.27pJ/b low-power optical receiver front-end in 65nm CMOS. In *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS) 2014*, Melbourne, Australia, 1–5 June 2014.
- [43] Takahashi, Y., Ito, D., Nakamura, M., Tsuchiya, A., Inoue, T., & Kishine, K. (2022). Low-power regulated CASCODE CMOS transimpedance amplifier with local feedback circuit. *Electronics*, 11(6), 854.
- [44] M. Dham, "2 to 4 Decoder," *PrepBytes Blog*, Jun. 16, 2023. <https://www.prepbytes.com/blog/digital-electronics/2-to-4-decoder/>