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A NEW DESIGN FOR COMPRESSION TECHNIQUE FOR TESTABILITY DESIGN

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ABSTRACT

With the advance in LSI/VLSI technology, the increasing inaccessiblity and density of the circuits and shortage of I/O ports for test purposes make testing more difficult and complex. This complexity in testing can be alleviated by making the design at Smallest-Repair-Replaceable-Unit (SRRU) level a testable design. The aim of the testable design concepts is to achieve, control, observation and isolation down to SRRU (chip) level. These concepts should be available by the construction of testability design to prevent the faulty propagation from one chip to another and to attain the highest degree of testing capability.

One of the techniques to achieve the testability design concepts is the compression technique. The established design for this technique has some problems which cannot be avoided, for example, it cannot provide isolation between the chips at SRRU level in TM (Test Mode), and at the same time to be used in system in OM (Operation Mode). Furthermore, the established design requires a much longer test application time. To alleviate the effects of these problems and to obtain more reliable results, a new design for compression technique will be proposed.

1) INTRODUCTION

Of the various testability-design approaches proposed so far, only the ECIPT [1] and the FCPA [2] can provide for isolation, control and observation of a chip's pad-bound N-inputs and outputs so as to make the chip testable in-system. The FCPA design has greater potentials than the HCPA [2], since it can provide isolation of the N-input through the added buffering SRLs and thus can in effect furnish an arrangement which can be made self-sufficient for testing.

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In the evolution toward incorporating in-system at-speed testability (ISAST) in system-parts, two main steps are necessary. The first is to gain access to the latches in the system-parts for their control and observation by using a latch-scanning arrangement (LSA) [3-5]; this alone is still insufficient for attaining the aim of ISAST. The second step is to gain access to the combinational networks (Ns) for their control and observation: and isolation is needed, at least for the control (at the N-inputs).

However, with LSI/VLSI and increasing circuit-densities, the number of tests needed for exercising an object-to-be-tested (OtbT) greatly increases. Although this number can be some what reduced (by adding switching at the I/O-ports of system-parts to extend access to the part's interior; i.e., by partitioning the OtbT, the single-cycle testing (with the lengthy scan-in and scan-out of test-data accompanying each test) proves too time-consuming and inefficient.

To overcome this problem, a concept that can be used is to provide means for internal pattern generation and response compaction for feed-and sinks that are within the OtbT (or close proximity to it). Thus, the scan-in and scan-out of data for each single-cycle test can be avoided and the time needed for latch-scanning can be greatly reduced.

2) INTERNAL PATTERN GENERATION AND RESPONSE COMPACTION

Many approaches have been proposed and used to implement this concept: they share the principle of using a pseudo-random-pattern generator for the source, or/and a pattern compactor for the sink. This section will discuss the essentials of these approaches. This group of approaches will be called here as "pseudo-random-pattern tests"- since these are rather loose and overly broad expressions. As a specific designation, "self-test" seems inadequate for three reasons:

(a) It is inexact, because testing should always be (and can only be) performed under control: strictly speaking no circuitry, especially not a system-part, can really "test itself". As will be seen, all so-called "self-tests" will actually need external controls for initialization (setting to known, definable states), start and stop, and result evaluation. There can be reduction in the controls from the external, but never a total elimination. A more fitting name may be "self-stimulated tests"; but this would not be entirely appropriate either, because it would allude only to the input stimulation for control, and the output compaction for observation.

(b) The PRPTs are only one of the possible forms of "self-tests". As will be seen also in the next subsection, "self-test" can be performed using not only pseudorandom, but also

determinstic, patterns.

(c) As for testability design, what would be most desirable, it is believed, is not really that systems and system-parts be capable of "self-testing" without control, but rather that they can be tested in-system and at-speed while under control.

Similarly, it seems obvious that "built-in-test" is also overly broad since, as was mentioned, "testability design" involves hardware design; i.e., the addition of circuits. Thus, in all testability-design; measures will be "built-in".

In essence, the main motivation in pursuing the PRPT is to reduce the costs of testing. As discussed earlier, with the OtbT not being easily accessible for testing and often of higher operational speeds than the test equipment available, feeding of stimuli to the OtbT and sensing the responses from it constitute increasingly difficult problems in LSI/VLSI testing. As testing "at-speed" becomes more and more important. it seems self-evident that since the test-interface is limited in data-transfer capability, testing must be done using stimulus-patterns supplied from a source that is within the test-object (or in close proximity to it), and letting the responses be collected by a sink that is also within (or close to) it.

Since the test-object normally does not contain a storage facility with large capacity, The stimulus-patterns obviously cannot all be stored ones, and the response collection cannot be simply capture and storage. By using on-site hardware-generated pseudorandom patterns (instead of stored precomputed ones) for the stimulus supply, it should be possible - besides achieving at-speed testing - to reduce the costs for the generation, storage and scan-in of test-patterns. On the other hand, by using on-site hardware-implemented pattern-compaction for the response acquisition, costs for the scan-out, storage and processing of test results can be decreased.

2.1) GENERATION OF PSEUDORANDOM PATTERN

The main method for generating pseudorandom patterns in PRPT is to use an arrangement called the "linear feedback shift register" (LFSR) [6]. The LFSR is a shift register with additional feedback connections via exclusive-OR (XOR) gate.

The patterns generated are said to be pseudorandom, since they are in a predetermined sequential order (dependent on the actual implementation and intialization) and hence are not truly random. The feedback is referred to as "linear", since it is associated with the implementation of "linear codes", and since the XOR-gates perform only "linear" operation ("modulo 2 additions") on the binary values. Combined with the shifting, the XOR-operations may be considered as performing a "modulo 2

division on polynomials", which is the basis of techniques for implementing what is known as "cyclic code" [7].

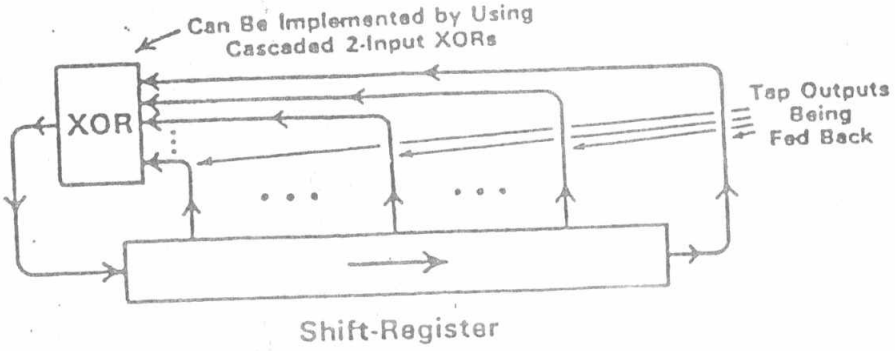

Figure 1 Basic structure of linear-feedback shift-register.

Figure 1 shows the basic structure of an LFSR. It consists of shift-register comprising a number of stages (bit-positions), with added feedback connections. Outputs of the last and some intermediate stages are tapped and fed back to the first stage via XOR-gates - the first and last stages being the leftmost and rightmost bit positions, respectively, if the register shifts left-to-right.

2.2) COMPACTION OF TEST-RESPONSE PATTERNS

The motivation in performing compaction on the response-patterns is, as mentioned earlier, to reduce the costs of testing. To circumvent the need for transmitting the test-responses immediately to the external tester for evalution to save time and storage expenditure thereby involved, a solution would be to capture and evaluate the responses within the object being tested. The aim is to make possible the execution of a long sequence of tests in rapid succession without needing to use large storage for collecting the successive test results. For this, the test responses need to be first obtained and then compacted so as to occupy less space. The compacted result will be a cumulative pattern for a long sequence of consecutively executed tests. For its comparison, only a single "expected result" needs to be computed and stored for use.

For the test-response compaction, mainly two methods can be used: counting [8] and compression (recursive compaction) [9]. In both cases, some preliminary evaluation of the test responses will be necessary, to extract some chracteristics that will be countable or representable by binary patterns.

In the case of counting, the characteristics being counted can be: the number of "1"'s transitions ("1"-to"0"-to-"1" changes), or "edges" (changes in one direction). For counting, conventional counter circuits can be used. These will not be discussed further here. Comparison (recursive compaction) refers to a process, by which a large amount of digital information can be reduced to a fixed small amount according to certain algorithms. Basically, it is a kind of encoding operation; and many of the techniques for implementing the "cyclic codes" can be applied here. As alluded to, the LFSR can be as the "core" in the circuitry for collecting and compressing test-response patterns. In combination with a single XOR-gate, the LFSR can provide a "single-input pattern-compressor" (SIPC); with multiple XORs, a "multiple-input pattern-compressor "(MIPC). The MIPC is most applicable, and it will be illustrated as follows.

2.2.1) MULTIPLE-INPUT PATTERN-COMPRESSOR (MIPC)

The basic structure of multiple-input pattern-compressor (MIPC) is shown in Figure 2 . The use of such a compressor was first reported in [10], [11] and [9]; in the last of these, it is referred to as a "multiple-input signature register" (MISR).

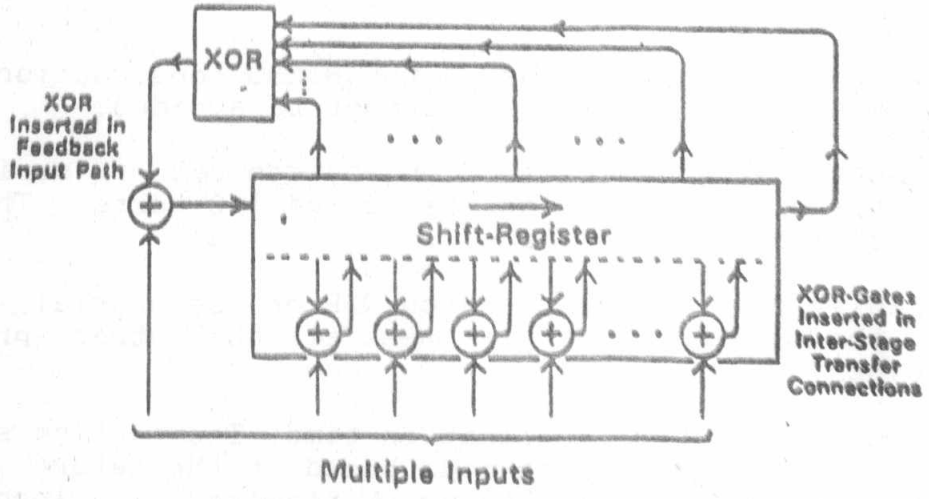

Figure 2 Basic structure of multiple-input pattern-compressor (MIPC) using an LFSR as core.

The MIPC is an arrangement in which, in addition to the

leftmost stage, each of the remaining stages of the LFSR will also receive a bit-stream input via an XOR-gate. In each test cycle, the output of each latch-stage will be XORed with a bit of an input-stream and shifted into the next stage to the right; the feedback input to the leftmost stage will also be XORed with an input-bit. Figure 3 gives an example for an MIPC using an LFSR-core based on the polynomial $x4+x+1$.

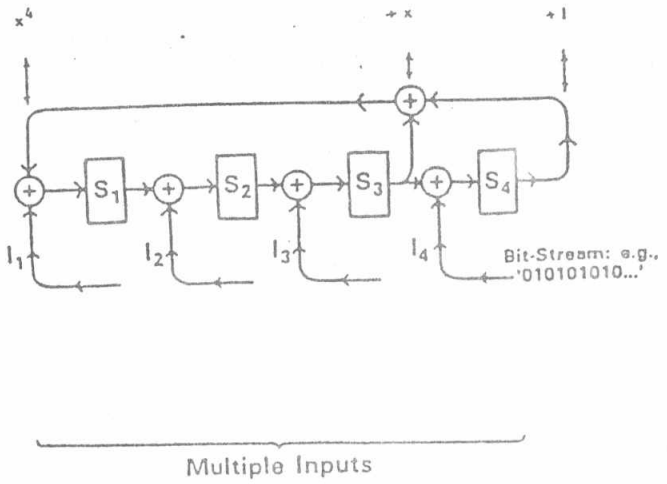

Figure 3 Example: 4-stage MIPC using LFSR-core based on x^4+x+1.

The use of a MIPC as PRPTs was reported in approaches called "autonomous testing" ([12], [13]) and "built-in logic block observation (BILBO)" ([9]). Of these, the paper on the BILBO which incorporate an interesting feature in addition to the use of a MIPC.

From the different modes of the BILBO construction (SIPC or MIPC), the following problems cannot be avoided:

i) The scan-path mode is based on the concept of serialising the data transfer to minimize the use of I/O ports. The main problems associated with it are:

* the faulty point nearest (latch O/P or sequential network O/P) to the scan-out port will mask all the other preceding faulty points.

* increasing of the test application time. The testing strategy associated with a scan-path mode based on the nature of the strobe-in strobe-out mechanism, requires a long test application time. Furthermore problems associated with this mode have been proposed in [14].

ii) The BILBO can be used as a response pattern generator when all inputs are set at "0", but in this case the BILBO cannot be used in the system in operation mode (OM). This means that,the BILBO construction cannot be able to provide the isolation

between the connecting chips on the module at test mode (TM).

To alleviate the preceding problems a new construction of the compression technique will be proposed.

3) NEW DESIGN FOR RESPONSE COMPACTION

Figure 4 shows a new design for response patterns compaction. Essentially, this design has multiple modes with more facilities than the BILBO design.
Shown in Figs. 5 (a) through 5 (e), there are five useful modes of operation, controlled by three mode control lines C1, C2 and C3 (same as in BILBO).

A BILBO new design construction (Fig. 5.d) can be defined by a set of state equations derived for each output Q:

$$Q_1 = [\overline{Q_3 \oplus Q_4}] \oplus I_1 \quad , \text{where } \oplus = \text{XOR, and}$$

$$Q_j = [\overline{Q}_{(j-1)} \oplus I_j] \quad , \text{where } j=2,3,4.$$

These equations describe the behaviour of the BILBO and new design techniques.

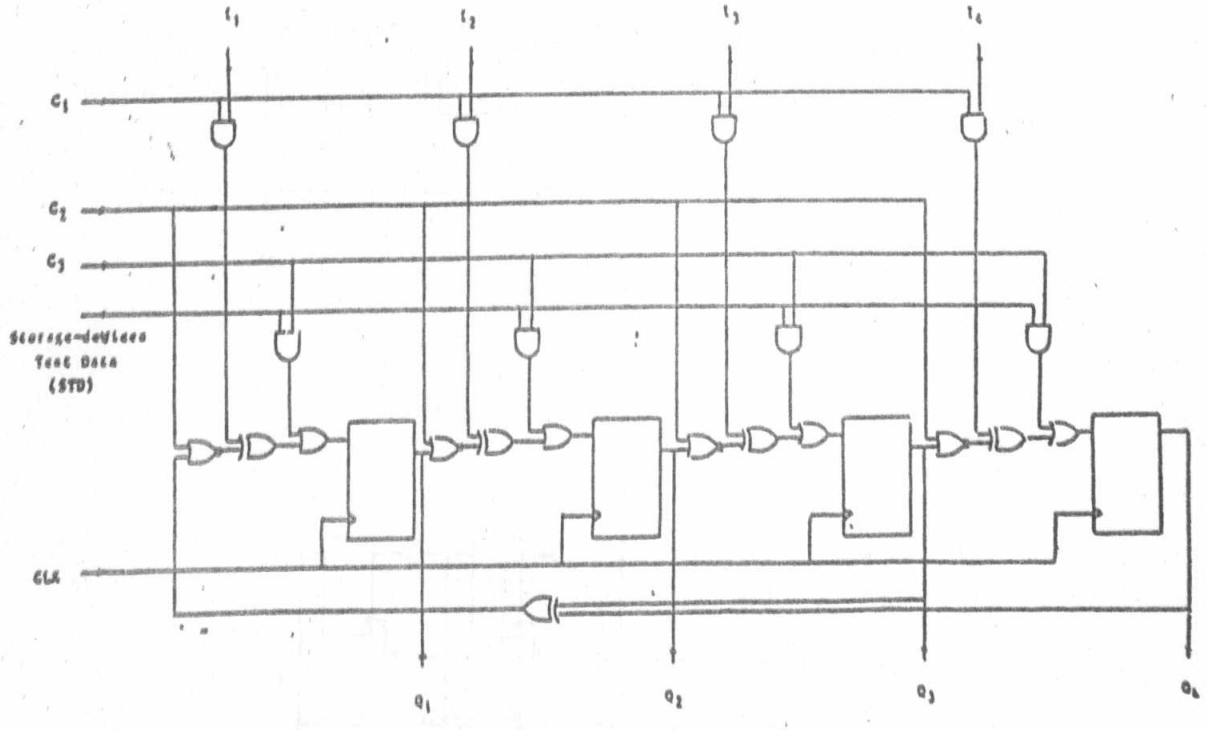

Figure 4 New design for response compression.

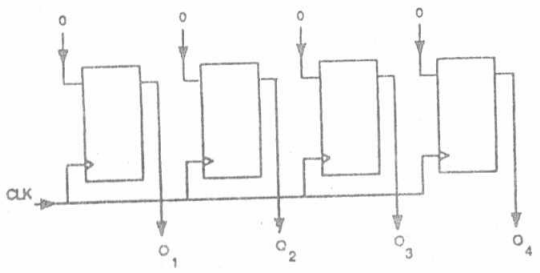

Figure 5(a) New design reset mode: C_1=0, C_2=1, C_3=0.

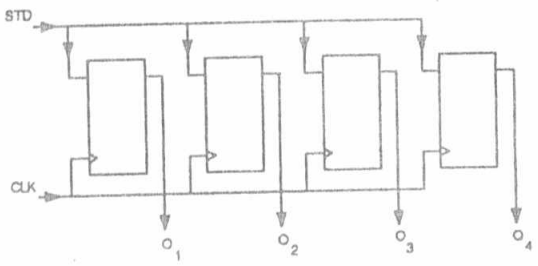

Figure 5(b) New design latch testing mode: C_1=0, C_2=1, C_3=1.

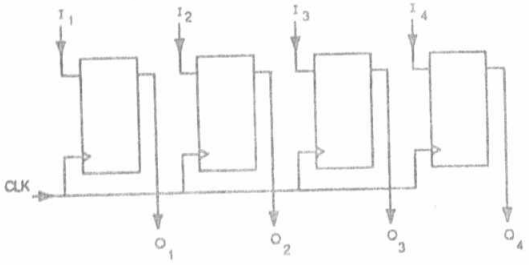

Figure 5(c) New design normal latch mode: C_1=1, C_2=1, C_3=0.

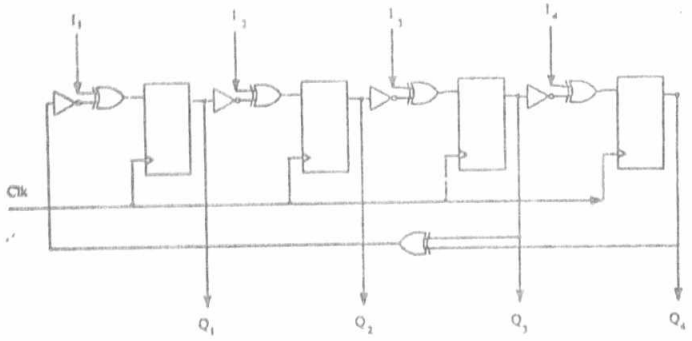

Figure 5(d) New design LFSR mode: C_1=1, C_2=0, C_3=0.

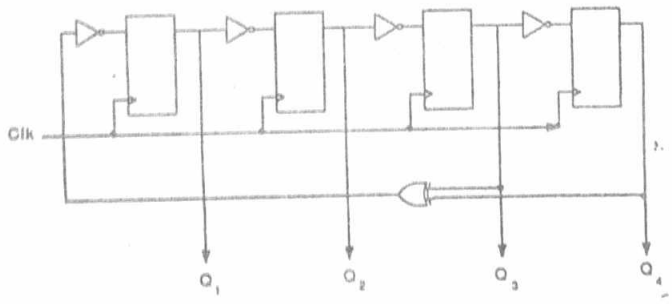

Figure 5(e) New design pseudo-random generator mode: C_1=0, C_2=0, C_3=0.

As discussed earlier, the problem of serialization of the data transfer associated with scan-path mode of BILBO design can be solved with the new design as shown in Fig 5 (b). Fig. 5 (b) shows that the stored stages can be observed individually, and the result of faulty node cannot emigrate from one node to another. Furthermore flushing "0"'s and "1"'s to test these stored stages as in BILBO are not required any more. Only a single "0" and "1" are required to test these stored states, (i.e., no flushing needed) enabling a saving in application test time.

The advantage of the new design (Fig. 5(e)), is that there is no restriction as with BILBO construction, and it also provides isolation between the chips (at the input pins) in generator mode without hardware overhead. LFSR mode must not be initialized with "0101" (lock-up pattern) in BILBO design or the new design - because in this case, the SR contents will remain "0101" through all shift cycles.

4) CONCLUSIONS

With the advances in LSI/VLSI, the increasing inaccessiblity of the circuits and shortage of I/O ports for test purposes, make testing more difficult and increase the testing costs to be an evergrowing portion of the total product cost. This complexity in testing LSI/VLSI designs can be reduced by making the design both a testable and diagnosable.

To achieve the above demand, the following requirements should be considered:

a) Divide large portions to smaller parts, which use repetitive test patterns.

b) Facilitating and simplifying test generation.

c) Minimising number of I/O ports created.

d) Minimising overall hardware and delay overheads of OtbT.

e) Avoiding errors due to faults in other parts from entering into the part being tested, thereby generating incorrect results.

f) Attaining the highest degree of testing capability at higher diagnosable levels.

In relating to the above requirements, the new design for response compression, proposed in this paper, alleviates the effect of the problems associated with the established design. Further advantages are, lower application test time and its use as a pseudo-random generator without any restriction to achieve the isolation between the chips at SRRU level.

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